OPTIMIZATION OF EMITTER LAYER IN N-TYPE BIFACIAL CRYSTALLINE SOLAR CELL

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

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IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
MICRO AND NANOTECHNOLOGY

MAY 2022

Approval of the thesis:

OPTIMIZATION OF EMITTER LAYER IN N-TYPE BIFACIAL CRYSTALLINE SOLAR CELL

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ABSTRACT

OPTIMIZATION OF EMITTER LAYER IN N-TYPE BIFACIAL CRYSTALLINE SOLAR CELL

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May 2022, 103 pages

P-type solar cells currently hold most of the market share in industrial solar cell fabrication statistics. NREL's highest efficiency record for p-type crystalline perc cells is 22.8%. However, there is an ever-increasing interest in n-type wafers due to the many advantages they have against p-type cells. According to the ITRPV's estimation, the n-type cell structures will be taking half the industry's share by 2031. Compared to p-type cells, n-type cells yield better efficiency and lifetime values, are not affected by boron-oxygen defect and light-induced degradation (LID). However, the processes of boron emitter doping and passivation in this cell type can be challenging. Also, a boron-rich layer (BRL) forms during the boron doping process. Due to the high density of inactive boron atoms, BRL acts as a high carrier recombination site. As a result, it is essential to effectively remove and replace it with another layer that effectively passivates the emitter surface. Therefore, the primary work of this thesis is to optimize the boron doping recipe resulting in uniformly doped emitter regions. Various thermal and chemical oxidation recipes were tested and optimized. Different passivation stack layers were also tested in

order to achieve the best imp V_{oc} results. The firing temperatures were optimized, aiming to achieve good contact resistivity values while preserving the imp V_{oc}.

Finally, the bifacial solar cell was produced utilizing the optimized values as a proof of concept. The fabricated cells have been characterized and analyzed with an efficiency of 18.2% and a V_{oc} of 0.631 V.

Keywords: Boron Emitter Doping, BRL Removal, N-type Solar Cell, Bifacial Solar Cell

ÖZ

N TİPİ ÇİFTYÜZEY KRİSTAL GÜNEŞ HÜCRESİNİN EMİTÖR KATMANI OPTİMİZASYONU

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Mayıs 2022, 103 sayfa

P tipi güneş hücreleri şu anda endüstriyel güneş hücresi üretiminde pazar payının çoğunu elinde tutmaktadır. NREL statistiğine göre, p tipi kristal perc hücreleri için en yüksek verimlilik rekoru %22.8'dır. Ancak n tipi güneş hücrelerine p tipi hücrelere karşı sahip oldukları birçok avantaj nedeniyle giderek artan bir ilgi söz konusudur. ITRPV'nin tahminine göre, n tipi hücre yapıları 2031 yılına kadar sektördeki payının yarısını alacaktır. P tipi hücrelerle karşılaştırıldığında n tipi hücreler daha iyi verimlilik ve ömür değerleri sağlar, boron oksijen kusurundan ve ışığa bağlı bozulmadan etkilenmezler. Ancak bu hücre tipinde boron emitör katkılama ve pasiflik işlemleri zorlayıcı olabilir. Ayrıca, boron katkılama işlemi sırasında boron bakımından zengin bir katman (BRL) oluşur. Aktif olmayan boron atomlarının yüksek yoğunluğundan dolayı BRL katmanı, yüksek rekombinasyonlu bir alana dönüşebilir. Bu yüzden, BRL katmanını etkili bir şekilde kaldırıp pasifleştiren başka bir katmanla değiştirmek önemlidir. Bu nedenle, bu tezin odak noktası, homojen bir emitör elde etmek için boron katkılama reçetesini optimize etmektir. Çeşitli termal ve kimyasal oksidasyon reçeteleri test edilmiş ve optimize edilmiştir. En iyi imp V_{oc}'yi elde etmek için farklı pasivasyon katmanları da test

edilmiştir. Ateşleme sıcaklıkları da optimize edilerek, imp V_{oc}'yi korurken iyi kontak direnci değerleri elde etmeyi amaçlamaktadır.

Son olarak, çift taraflı güneş hucreleri, optimize edilmiş değerleri kullanılarak bir konsept kanıtı olarak üretilmiştir. üretilen hücreler %18.2'lik bir verimlilik ve 0.631 V'lik bir V_{oc} elde etmiştir.

Anahtar Kelimeler: Boron Emitör Katkılama, BRL Kaldırma, N Tipi Güneş Hücresi, Çiftyüzey Güneş Hücresi

To my amazing mother, Faranak Salehi

and my family…

ACKNOWLEDGMENTS

I would like to thank my dear advisor Prof. Dr. Raşit Turan for his endless support and for giving me the opportunity to work at the GÜNAM research center. I want to thank my supervisor E. Hande ÇİFTPINAR for her kind assistance and consultation during my research. I would like to acknowledge Ahmet Emin Keçeci and Ateşcan Aliefendioğlu and the rest of the GÜNAM family for their helpful assistance during my research work. I would also like to thank my dear sister and coworker Arghavan Salimi for always supporting me. I would also like to thank my mom and dad for always being there for me and providing both financial and emotional support throughout my studies here.

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LIST OF ABBREVIATIONS

ABBREVIATIONS

4PP	Four Point Probe
ALD	Atomic Layer Deposition
AM	Air Mass
APCVD	Atmospheric Pressure Chemical Vapor Deposition
ARC	Anti-Reflection Coating
BRL	Boron Rich Layer
BSF	Back Surface Field
BSG	Borosilicate Glass
CTLM	Circular Transfer Length Method
CVD	Chemical Vapor Deposition
ECV	Electrochemical Capacitance-Voltage
FCA	Free Carrier Absorption

FEP	Field-Effect Passivation
ICP	Inductively Coupled Plasma
ITRPV	International Technology Roadmap for Photovoltaic
LED	Light Emitting Diode
LID	Light Induced Degradation
NREL	National Renewable Energy Laboratory
PECVD	Plasma Enhanced Chemical Vapor Deposition
PID	Potential Induced Degradation
PLI	Photoluminescence Inspection
PV	Photovoltaic
QSS	Quasi Steady State
SRH	Shockley Reed Hall
TLM	Transfer Length Method

LIST OF SYMBOLS

SYMBOLS

H	Hydrogen
He	Helium
V_{oc}	Open Circuit Voltage
Eg	Band gap
CB	Conduction band
VB	Valence band
Si	Silicon
GaAs	Gallium Arsenide
Ge	Germanium
Ec	Band Energy of the conduction Band
Ev	Band Energy of the Valence Band
Eg	Band gap

FF	Fill Factor
J_{sc}	Short Circuit Current Density
n	Number of free electrons in conduction band
p	Number of holes in valence band
η	efficiency

CHAPTER 1

INTRODUCTION

1.1 Using The Sun as a Source of Energy

Sun is undoubtedly the most important source of energy for our planet earth. Every day during the daytime, it emanates a considerable quantity of heat and sunrays toward us. This infinite amount of energy that can be used with no complications is essential for the survival of all living forms [1]. The main advantage that sets solar energy aside from other sources of power is that sun rays provided by the sun can be turned into electricity with the help of thin cells made out of various kinds of materials called solar cells [2][3]. But before going deeper into the working mechanism of this photovoltage cell, It is better to understand how this solar energy is actually formed.

This star, which we call the sun, comprises an enormous spherical atmosphere of gasses that mainly consists of hydrogen and helium. Through a phenomenon called Nuclear fusion reaction, the hydrogen atomic nuclei are fused to form the helium atomic nuclei and also subatomic elements. The variation in the atomic mass of the initial hydrogen nuclei and the resulting helium nuclei is exhibited in the form of releasing additional energy as depicted in eq.1.1 and eq.1.2.

$$ {}_{1}^{2}H + {}_{1}^{2}H \rightarrow {}_{2}^{3}He + {}_{0}^{1}n + 3.27MeV \qquad (1.1) $$

$$ {}_{1}^{2}H + {}_{1}^{3}H \rightarrow {}_{2}^{4}He + {}_{0}^{1}n + 17.59\ MeV \qquad (1.2) $$

During this fusion process, four hydrogen atoms combine to form one helium atom with a loss of mass which is radiated as thermal energy [1][3]. Unlike fossil fuel energies produced on earth, This energy is immaculate and does not contain any polluting substances, and it also does not create any sort of noise pollution[4].

The main benefit this renewable energy holds against the other primary energy sources is its extreme accessibility; regardless of living in urban or rural areas, people can make use of this energy for various fields, from domestic use to big scale industrial facilities. Even though solar energy is available for an unlimited amount of usage and is completely free of charge, transforming this solar energy into something usable for human-made appliances and technologies is not.

The manufacturing of the cells can be costly. In fact, with the increased variety of renewable energy sources, there has been a competition to yield the lowest cost. Therefore, optimizing the financial part of the process has also gained a lot of importance [5]. Of course, This green and renewable energy source has its downsides as well. The limited daylight hours make the process tricky as it would be impossible to supply electricity at night. A solution to this problem is utilizing batteries to store the surpluses of the produced electricity to use at night.

There is also the possibility of lack of sunlight due to undesired weather conditions. Overall, the amount of sunlight reaching one particular area depends on many factors, such as the geographical position and distance from the equator and what season of the year it is [5]. All this limitation in harvesting solar energy makes it vital to focus more on increasing the overall efficiency of the solar panels.

1.2 The History of Solar Energy

The story of humankind’s dependence on energy goes as far as history itself. It all started with the invention of fire through burning wood and later evolved into using natural gas and other fossil fuels. However, the earth's primary energy source is and always will be the sun. The sun provides the necessary light and heat for the survival of all living beings and, in a way, is the foundation of all the other energy sources. The plants absorb the sunlight and, through the chemical process called

photosynthesis, turn it into chemical energy. The chemical energy forms the plants that are the primary nutritional source of other living beings. All these aforementioned sources of carbon then become the base for woods, coals, and all the fossil fuels.

The hydropower is also accommodated by the sun. The water on the earth's surface evaporates as a result of exposure to sunbeams. It then returns in the form of rain on mountain tops and, by utilizing gravity, forms the fast-running bodies of water such as rivers providing the power to store the energy.

The wind used by windmills and turbines is also a byproduct of the sun since the wind is created by the movement of air resulting from a difference in its temperature. With the exception of geothermal, nuclear, and tidal energies, almost all the other sources of energy depend on the sun. Which raises the question of why not store the sun's energy directly?

The first person to uncover the ability to produce electricity from light was Edmond Becquerel. In 1839, While experimenting with cells made out of metal electrodes, he accidentally found that the cell generates more electricity under sunlight [6]. However, the first person to ever make a working solar cell was an American called Charles Fritz. By working on the previously discovered phenomenon by Willoughby Smith that selenium displays a photovoltaic effect, he was able to produce the first-ever solar cell was made out of selenium in 1883 in New york city. Despite having very idealistic hopes for the future of his discovery, Mr. Fritts's solar panels were only able to produce electricity with an efficiency of 1 percent [7]. Later on, a professor called Augustin Mouchot began to do research on how to harvest power from solar energy in order to find a better alternative for fossil fuels. He was able to come up with a device called the sun engine. The system worked by heating water via concentrated sun rays and was a type of steam engine.

However, since, at the time, fossil fuels were abundant and easy to utilize, he was not able to receive support from his country's government to further develop his work.

One of the revolutionary discoveries in solar energy utilization is perhaps the discovery made by an American called Edward Weston in 1888. He took a different

path from his peers by producing electricity by employing the Seebeck phenomenon [8]. According to this phenomenon, the variance in temperature between two different semiconductors results in a potential difference that can be utilized in extracting electricity. As is shown in the figure.1.1, Weston focused the solar energy on one point using a lens and then used it as a source of heat to cause a variation in the temperature of the metal pieces and generate electricity; the produced electricity will be stored and then employed to turn the motor [9].

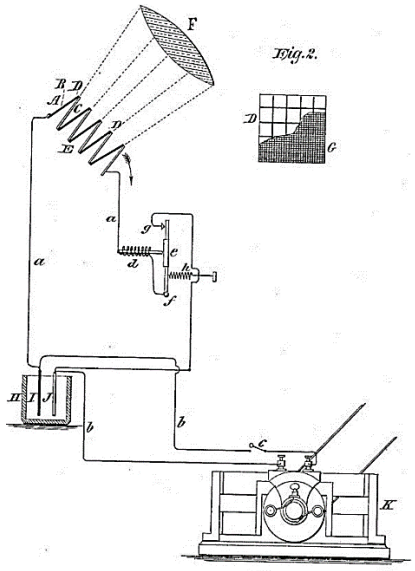

Figure 1.1. Edward Weston's thermopile-based apparatus for utilizing solar radiant energy. (Adopted from [9].)

The invention of the silicon cell type was first started when Heinrich Hertz encountered the photoelectric phenomenon. He observed that when certain radiation like the sunbeams reaches a material, it results in the carrier's (electrons) emission. This phenomenon was later comprehensively theorized by Albert Einstein in 1921. As this was a major scientific discovery, he was awarded the physics Nobel prize that year [10].

But the first person to make a solar cell based on this phenomenon was a physicist called Alexander Stoletov [11].

One of the important developments that were a key point in manufacturing solar cells was the crystalization technique which is now known to us as the Czochralski method. This method was developed by Jan Czochralski in the year 1918 [12].
The solar cell made out of silicon as we know it today was invented Years later.
All these innovations in science led to the invention of the first-ever silicon cell in the United States in 1954 [13]. Daryl Chapin, Calvin Fuller, and Gerald Pearson, who were scientists from the Bell Labs, a renowned research center, made this invention. The first cell was an n-type silicon cell doped with boron to create the p-type emitter on top of it. This cell was able to yield an efficiency of 6%.
The utilization of silicon in producing solar cells was a major breakthrough since the abundance of silicon makes it easy and affordable to mass-produce. And it was the stepping stone for the many modern variations of the silicon solar cells that we know today.

1.3 The Working Mechanism of Solar Cell

1.3.1 Types of Materials Used in the Photovoltage Industry

Choosing the materials used in different solar cell layers probably has the most significant role in determining the efficiency of the produced cell. To select the best fitting material for a set layer, one must first be familiar with different types of materials. Based on their resistivity, the materials can be separated into three main groups: conductors, semiconductors, and insulators.

1.3.1.1 Conductors

conductors have very low resistivity values, meaning the electricity can pass through them easily. The bandgap energy (E_g) of a material is the difference of energy levels between the valence band and the conduction band energy. E_g determines how easily the electrons in the valence band can jump into the conductance band. In the case of

a conductor, the two bands are overlapping ($E_g = 0$) so when slightly excited, the valence electrons would elevate to the conduction band. There is no energy difference between the two energy bands in an ideal conductor.

Most metals are good conductors. Additionally, salts can also conduct electricity when dissolved. The conducting agents, in this case, are the ions that are set free after dissolving.

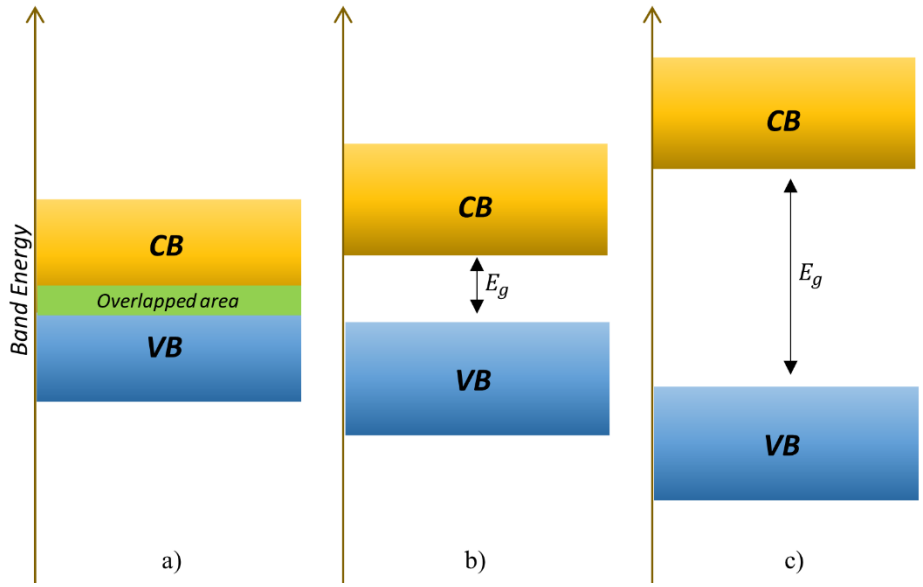

Figure 1.2. Energy diagram of each material type. a) Conductors, b) semiconductors, and c) Insulators.

1.3.1.2 Insulator

Unlike conductors, insolating materials do not conduct electricity efficiently. The valence band is strongly bonded with the nuclei, making it difficult for the carriers to get excited. The difference between valence and conduction band is so big that it is virtually impossible for the conduction band to be filled with free electrons unless exposed to a significant amount of voltage (breakdown voltage) strong enough to detach all the electrons from their nuclei. Insulators are usually compound materials.

1.3.1.3 Semiconductors

Semiconductors are the middle ground for the two abovementioned materials; they contain features from both material types. Therefore, they can be used where controlled conductivity is required, making them desirable in fabricating state-of-the-art technologies. Unlike conductors, there is a bandgap in semiconductors; however, it is smaller. Also, the valence band is not fully occupied here. When external energy is absorbed, the valence electron will be able to cross the bandgap and go to the conduction band, leaving behind positive charge carriers, i.e., holes. Under absolute zero temperature, semiconductors behave just like insulators, and with the increase in heat, their conductivity also increases. Both single element and compound materials can be semiconductors. Silicon (Si), Gallium Arsenide (GaAs), and Germanium (Ge) are one of the most used semiconductors in the photovoltage industry. Semiconductors can be grouped into two: intrinsic and extrinsic semiconductors.

Intrinsic semiconductors are the neutral form. In this type of semiconductor, no impurity is added to the material, and only one kind of material is used. Intrinsic semiconductors are usually poor conductors and are not widely used in the industry. However, the amount of conductivity is altered with the temperature change. The number of free electrons and holes is equal in an intrinsic semiconductor. The reason why Intrinsic materials Have poor conductivity is the elements being tetravalent. Each atom makes a covalent bond with its nearby atoms, making a solid and stable bond between each atom's four outer layer electrons. Figure 1.3 depicts the atomic structure of intrinsic crystalline silicon.

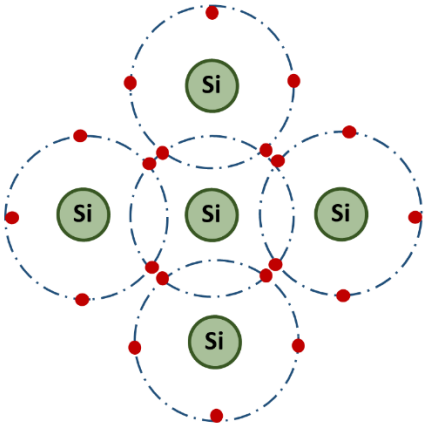

Figure 1.3. Atomic structure of intrinsic silicon.

However, this stability is corrupted when a different element (impurity) is introduced to this structure. The resulting semiconductor has way better conductivity that can be controlled by the amount of impurity injected into the structure and by the temperature. Depending on whether pentavalent or trivalent elements are used in the doping process, the extrinsic semiconductors can be further divided into two groups:

I. P-Type Semiconductors

If the material chosen for doping has three outer layer electrons (trivalent material), then the extrinsic semiconductor will become p-type. When an element with three valence electrons enters an intrinsic semiconductor, it disrupts the previous existing bonds and forms three covalent bonds. Still, one electron remains unattached, creating a hole instead. These additional holes break the equilibrium between the number of electrons and holes, making the holes majority carriers, and the electrons will become the minority carrier. The impurity atom (also called the acceptor atom) accepts the extra unbonded electrons in an energy level situated near the valence band called the acceptor band. Figure 1.4 depicts an atomic structure of boron-doped crystalline silicon.

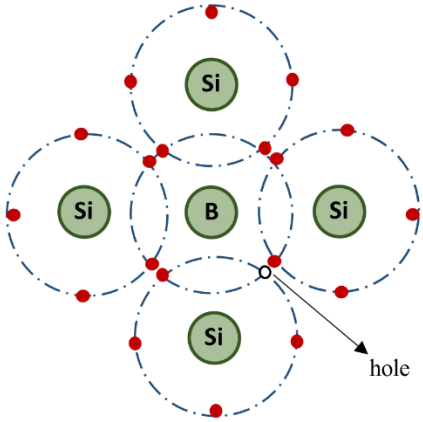

Figure 1.4. Atomic structure of p-type silicon.

II. N-type Semiconductors

In the case of pentavalent doping, the intrinsic semiconductor will end up with an extra electron. When the doping takes place, four electrons of the outer orbit of the dopants covalently bond with the electrons of four nearby atoms leaving the fifth electron unbonded. This unattached free-electron acts as a donor electron positioned in an energy band just below the conduction band. With the slightest excitation, they will be elevated to the upper level, increasing the conductivity of the semiconductor. Here the electrons are the majority carrier, and the holes are the minority carriers. Figure 1.5 depicts an atomic structure of phosphorus-doped crystalline silicon.

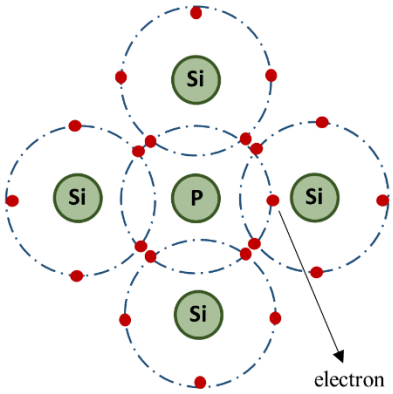

Figure 1.5. Atomic structure of n-type silicon.

1.3.2 The Formation of p-n Junction

When an intrinsic material is doped with both p-type and n-type material, a junction forms between them. As mentioned earlier, n-type material has a higher electron population, and p-type material has a higher positive charge. This imbalance in free majority carrier density causes the free carriers near the junction to travel to the other side. As each carrier is bonded with a fixed opposite charge inside the material, an area containing these fixed charges will form at the junction. This will create an electric field directed in the opposite direction of the majority carrier flow. The formed area is called the depletion region because it is completely depleted of any free carriers due to the opposite electric flow. For solar cells, the width of this layer is insignificant compared to the whole bulk of the device. Figure 1.6 shows this depletion region.

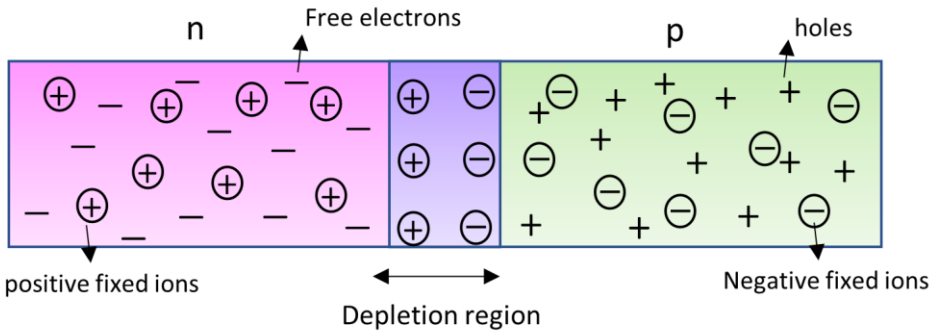

Figure 1.6. The formation of the depletion region in the p-n junction.

This depletion area will act as a barrier, creating a build-in voltage in the junction, which is one of the critical factors of a working solar cell. However, Some majority carriers with enough strength will diffuse through despite the current. These carriers will pass through the other side of the junction and, in doing so, will create another current called the diffusion current. This current is way smaller than the junction current but can increase if the temperature increases or a forward bias is applied to the device. Also, the minority carriers generated close to the junction will be pulled into the depletion area since the direction of the minority carrier movement and the electric field there are aligned. This carrier movement is called drift. At equilibrium, the drift and diffusion movements are evened out.

1.3.3 Energy Band Bending

The Fermi level is defined as the highest energy level the negative carrier of an intrinsic semiconductor can reach at a temperature of 0 kelvin. For an undoped semiconductor, it is stated at an equal distance from the conduction and the valence band. However, as we dope the semiconductor, the band positions change. In the n-type semiconductor, the E_c and E_v are positioned at a lower energy level than the p-type semiconductors. This results in the bending of the energy bands at the junction area. Figure 1.7 depicts the band-bending phenomenon.

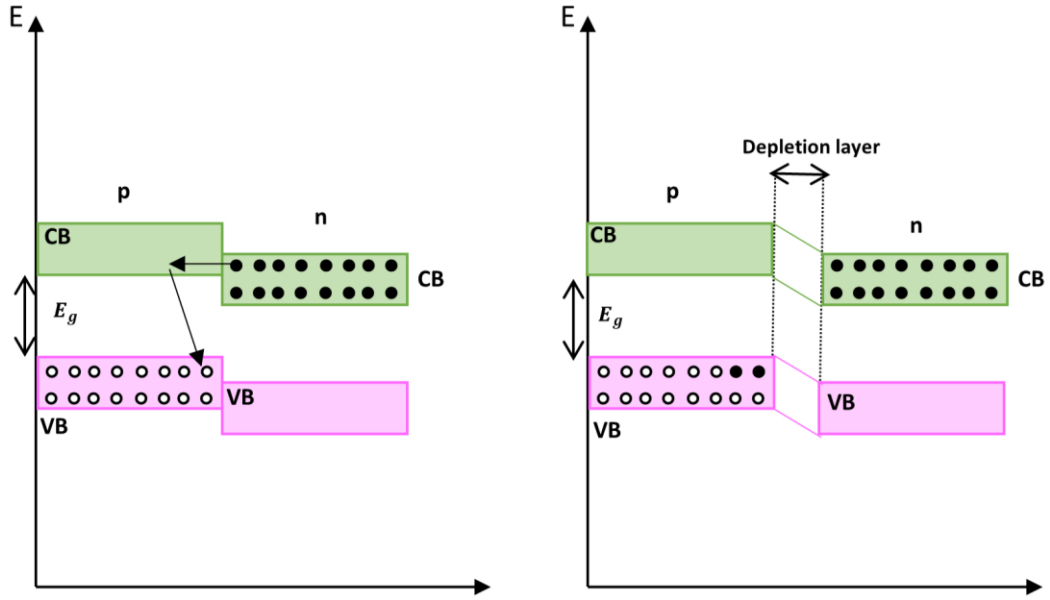

Figure 1.7. The energy band diagram and depletion region formation of the p-n junction.

Forming this p-n Junction and the Voltage barrier is the initial step of fabricating a solar cell.

1.3.4 Formation of Electron-Hole Pairs

The mechanism behind the Solar cell's ability to transform a photon into electricity lies in a phenomenon called the photoelectric effect, which results in the generation of electrons and holes as a pair. Due to this generated pair's separation, the electricity is produced. The incoming photon needs to fulfill an energy requirement for these pairs to form. if the photon energy (E_p) is lower than the E_g, the photon would simply be transmitted without absorption. E_p must be equal to or higher than the E_g Which in the case of a silicon-based solar cell is 1.11 eV [14]. If this is the case, the absorbed energy will cause an electron in the valence band to be elevated to the conduction band. This electron, together with its absence in the valence band also known as hole, will form the electron-hole pair. Figure 1.8 shows the reaction of electrons in the valence band upon contact with rays with varying E_p.

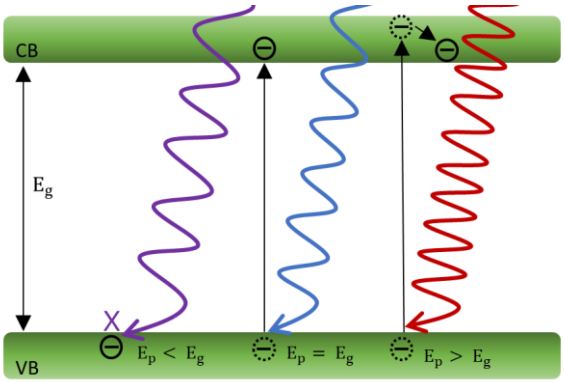

Figure 1.8. Carrier generation caused by the energy transmission from the incident photon to the carriers in the valence band.

The photogeneration process is more complicated for silicon, an indirect bandgap material. Unlike the direct bandgap materials, here the E_v and E_c are not positioned in the same level of momentum space in the dispersion graph. Therefore, the excitation of an electron requires additional momentum provided by a phonon.

The details of the difference between direct and indirect bandgaps will be discussed fully in section 1.3.2.1.

in the neutral condition, the charge carrier density is defined as:

$$n_i^2 = np \tag{1.3}$$

where the n_i stands for intrinsic carrier density. Carrier masses of electrons and holes can respectively be defined as:

$$n = n_0 = N_c e^{\frac{E_f - E_c}{K_B T}} \tag{1.4}$$

And

$$p = p_0 = N_v e^{\frac{E_v - E_f}{K_B T}} \tag{1.5}$$

Where the N_v and N_c stands for the carrier densities of valence and conduction band, E_f is the Fermi energy and K_B is the Boltzmann constant.

When put under illumination, as the aforementioned photogeneration phenomenon takes place, the carrier masses are redefined as:

$$n_i = \sqrt{N_c N_v} e^{\frac{E_v - E_c}{2K_B T}} \tag{1.6}$$

And

$$n = n_0 + \Delta n = N_c e^{\frac{E_{fn} - E_c}{K_B T}} \tag{1.7}$$

And

$$p = p_0 + \Delta p = N_v e^{\frac{E_v - E_{fp}}{K_B T}} \tag{1.8}$$

The Δn and Δp are the additional carriers absorbed in the illumination process. under nonequilibrium, the Fermi level of electron and holes are split into two as new charges are generated in the semiconductor. E_{fn} and E_{fp} are respectively the electron and hole's quasi-Fermi levels. These levels are critical in solar cell manufacturing as they determine the highest voltage produced by the cell.

So the implied voltage ($imp\ V$) of the semiconductor is defined as:

$$impV = \frac{E_{fn} - E_{fp}}{q} = \frac{k_B T}{q} \ln\left(\frac{(n_0 + \Delta n)(p_0 + \Delta p)}{n_i^2}\right) \tag{1.9}$$

In reality, however, many carriers are recombined due to the recombination losses, so the produced voltage is usually way smaller than the amount calculated by the equation above.

1.3.5 The Separation and Collection of Electron-Hole Pairs

In the next step, the generated carriers must be separated to get collected by the metal carrier collectors located on either side of the semiconductor.

Therefore, a force is needed to separate these carriers and sweep them to the collecting ends.

The probability of the created pair contributing to the generated current depends on the distance of the generated pair to the junction. If the pair is created too far from the junction, the minority carriers will be recombined before reaching the other end of the junction. The minority carrier's lifetime is how far in distance it can travel before getting recombined. When the generated minority carrier passes through the junction due to drift, it will become a majority carrier and will be collected by the metal collectors connected to an electrical circuit.

1.4 Understanding The Solar Radiance

not all of the solar energy emitted from the sun’s surface will reach the earth’s surface. The term Air Mass (AM) is used when dealing with solar cell technology to identify the amount of solar power received at a set wavelength spectrum. It is defined as the distance the sunray travels to reach the earth's surface to the shortest possible distance between the two locations and is shown as:

$$AM = \frac{1}{\cos(\theta)} \tag{1.10}$$

Where θ is the angle between the two distances. Figure 1.9 depicts the sun's spectral irradiance at different angles. AM 0 is also known as extraterrestrial irradiance and is the radiance received outside the atmosphere. Unlike the extraterrestrial radiances, which mostly remain unaffected, Terrestrial irradiance varies depending on environmental factors such as air pollution or climate-related factors such as rain or clouds covering the atmosphere. Also, it is affected by the seasonal change due to alterations in the day's length throughout the seasons. AM1.5 is the standard air mass for when the θ = 48.2°. And can be sorted into two groups: direct (only direct sunlight) and global (direct and scattered sunlight). The AM1.5 is mostly used in calculations and is rounded up to 1000 W/m^2 for convenience.

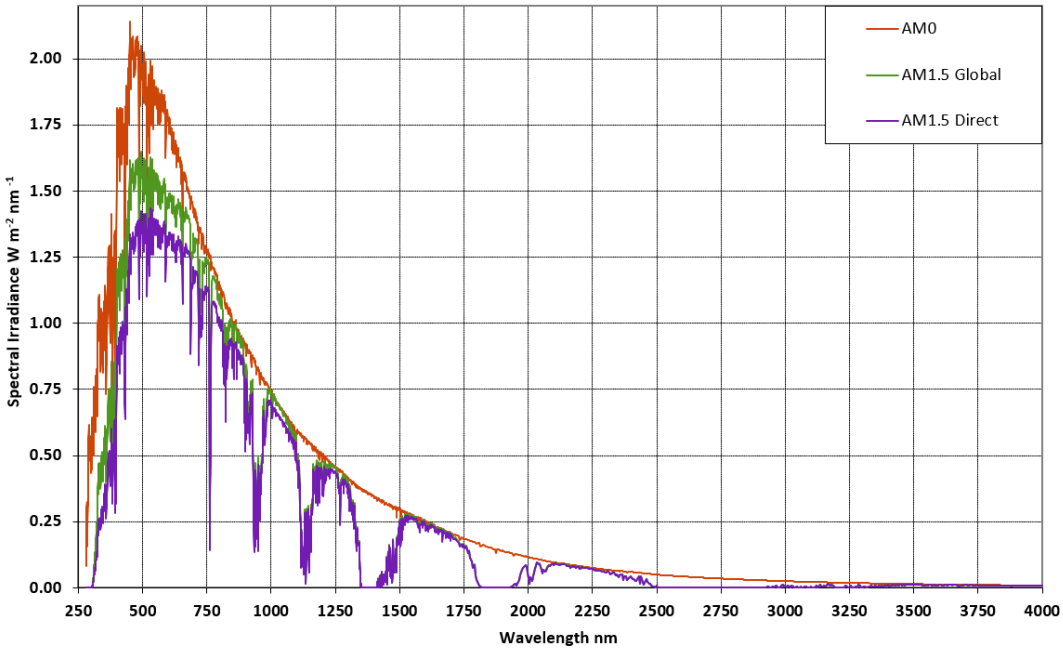

Figure 1.9. Sun's spectral irradiance (data retrieved from [15]).

1.5 N-type Solar Cells

In recent years, n-type wafers have regained popularity due to their many advantages compared to p-type wafers. These advantages make them a better material for the production of industrial solar cells. One of the main benefits of using an n-type substrate is the elimination of light-induced degradation (LID) which is one of the main causes of lifetime loss in p-type cells. The boron-oxygen pairs that form in the solar cell bulk are reported to be the reason behind this loss. Another issue is the impurities such as interstitial Iron (Fe) atoms that mostly recombine with the electrons. Since, contrary to the p-type cells, the minority carriers in n-type cells are the positive carriers (holes), n-type cells are not affected by the impurities as much as p-type cell structures.

Moreover, utilizing a back surface field (BSF) doped with phosphorus for passivation purposes can lead to higher efficiencies. The cell can also be utilized conveniently as a bifacial cell type offering even higher efficiencies than the mono facial cell types.

Owing to the aforementioned benefits, the n-type cell structure is gaining popularity in the industry.

For now, the market is mainly dominated by p-type wafers. However, according to the predictions of the 2021 issue of the international technology road map for photovoltaics (ITRPV), in almost ten years, the use of n-type silicon wafers will be equal to the p-type wafers [16].

The biggest challenge in manufacturing n-type solar cells is to reduce the effect of losses.

1.6 Reasons Behind the Losses

The two main components that directly contribute to building the overall efficiency of a properly working solar cell are the number of sun rays that get permeated and absorbed into the solar cell and the number of electron and hole pairs that are produced as a result. Therefore, any disruption in these two mechanisms will result in losses. These losses are grossly divided into three parts. Losses related to the reflection or transmission of the photons entering the cell surface are titled optical losses, The recombination loss that happens due to the recombination of the electron and hole pairs that would otherwise be separated and collected at the two ends of the cell , and finally, the losses that occur due to the resistances that exist in different layers of the cell called the resistivity losses.

1.6.1 Optical Losses

Incident photons that fail to get absorbed and contribute to the electron-hole production will be counted as culprits in this category of losses. To go through it more thoroughly, causes of Optical losses are divided into subsections:

1.6.1.1 Reflection of the Surface

Some of the incident photons get reflected after hitting the cell's surface. In order to incorporate these lost photons back into the solar cell, various methods have been used. For silicon cells, the surface can be textured either with the help of laser or chemical treatments, making the otherwise smooth surface indented with pyramid shapes. This retextured surface acts as a physical trap sight by affecting the angle at which the light reflects and thus increasing the chances of the light hitting the surface more than once and getting absorbed. On top of this texturing method, coating the surface with a layer of anti-reflection dielectric substance is another way to decrease the reflection even more. This anti-reflection coating (ARC) material is chosen so that its refractive index fits the equation below; n_1, n_2 and n_3 are, respectively, the refractive indexes of the area surrounding the cell structure, ARC material, and the original substrate of the cell.

$$n_2 = \text{SQRT}\ (n_1 . n_3) \tag{1.10}$$

This means that the light reflected from the outer surface of the ARC and the light reflected from its interface with the layer below it will collide destructively, and the resulting reflection will be zero.

The optimal thickness of the ARC for total destructive interference of the incident light can be computed as shown in eq 1.11., λ_{in} being the arriving light's wavelength:

$$d_{ARC} = \frac{\lambda_{in}}{4 . n_{ARC}} \tag{1.11}$$

For a silicon solar cell to fit the requirements in eq 1.11., the ARC material must have a refractive index of approximately 2. Therefore, hydrogenated silicon nitride (SiN_x: H) is mainly used as an ARC layer. Since the highest photon concentration

for the solar irradiance is in the wavelength of 600 nm, the optimal material thickness according to eq 1.12. is 75nm [17].

1.6.1.2 Transmission of Light

For a photon to contribute to the production of electron-hole pairs, it needs to be absorbed by the cell. The absorption coefficient of the material shows how much the photon with a specific wavelength has to travel in the semiconductor before getting absorbed by the material. Si has a low absorption coefficient, meaning that photons with longer wavelengths have a lower chance of absorption, especially in thinner wafers. Si also has an indirect bandgap, making the absorption process somewhat challenging [17]. In recent years, the production aim was to narrow the cells as much as possible to cut down on production and material expenses, and this has primarily affected the efficiency of cells [18]. Therefore, several methods have been incorporated to reduce transmission losses. One way is to use a full metallization at the backside. The metal at the back stops the photon transmission. however, it also acts as a recombination site and increases the cell's J_0 value. A better alternative would be to use a passivation layer at the back to fully passivate the backside. On top of decreasing the backside recombination, this layer adds to the overall thickness of the cell, and also because of the change in medium and the refractive index, the photons have a higher chance of reflecting back and ultimately being absorbed. The texturing on the rear side of the cell has a good impact on the reflectivity qualities of the back side.

1.6.1.3 The Surface Shading

Due to the working mechanism of the solar cell, the metal bars and fingers that are in charge of collecting the electron-hole pairs need to be located on the cell's surface. Naturally, this blocks the sun rays from penetrating the cell and results in significant

loss due to shading. The space blocked by metallization for a conventional cell type constitutes around 4 to 8 percent of the front surface.

Reducing the number of metallization fingers will effectively reduce the shading; however, this will raise the problem of the series resistance losses.

1.6.1.4 Ineffective (Parasitic) Absorption

Any type of light absorption that does not contribute to the production of electron and hole pairs is considered parasitic absorption. The refractive index consists of 2 parts: a real part and an imaginary part. The real part is the fraction of the speed of light in a vacuum (3x10^8 m/s) to the phase velocity of an electromagnetic wave in the set medium, and the imaginary part is associated with the absorption coefficient. Eq 1.12. shows the equation for the refractive index of a set wavelength. m stands for the total refractive index, while m_r and m_i are respectively the real and imaginary parts of the refractive index.

$$m(\lambda) = m_r(\lambda) + im_i(\lambda) \qquad (1.12)$$

Materials that only have a real part of the refractive index scatter the light that penetrates them. However, if the imaginary part of a material's refractive index is substantial, some absorption will occur. The ani-reflection layer initially acts as an agent for reducing the reflection. However, some of the light can be absorbed by the ARC layer itself if the material has a significant m_i Value. In the case of materials utilized in this thesis work, such as Al_2O_3, Si_3N_4 and SiO_2, the parasitic absorption is trivial. One of the agents contributing to parasitic absorption is free carrier absorption (FCA). In this phenomenon, rather than producing the desirable electron-hole pairs, the absorbed light transfers its energy to the electrons in the conduction band or the holes in the valence band and raises them to a higher sub-band within the same band.

1.6.2 Recombination Losses

There are three main types of recombination: band to band recombination (radiation recombination), Auger recombination, and defect recombination.

1.6.2.1 Band to Band Recombination

This recombination mechanism will happen due to the descendance of an electron from the conduction band to the valance band. As a result, a relatively weak photon will be released that passes through the semiconductor unabsorbed since it's comparatively close in terms of energy to the semiconductor's bandgap. This phenomenon mainly occurs in cells made with semiconductors with direct bandgaps such as GaAs. Since most solar cells are made out of silicon with an indirect bandgap, this recombination phenomenon isn't common and can be neglected in silicon solar cells. The reason behind the lower radiative recombination probability in indirect bandgaps lies in the difference in momentum between the two bands.

1.6.2.1.1 Direct and Indirect Bandgaps

In direct bandgaps, the valance band falls right under the conduction band, and both bands have the same value for momentum. This means that an electron can simply drop to the valance band by losing energy in the form of a photon. Because of this feature, materials with direct bandgaps are usually chosen to be utilized in the manufacturing of lasers or light-emitting diodes (LED). However, in the case of indirect bandgaps, there is a difference in the momentum value. This means that simply losing energy in the form of a photon is not enough for the electron to transfer to the valance band maximum. It also needs to fulfill the momentum change required for the drop by losing energy in the form of a phonon. Another solution for transition is through the defect states between the two bands. Figure 1.10 depicts the energy-momentum diagram.

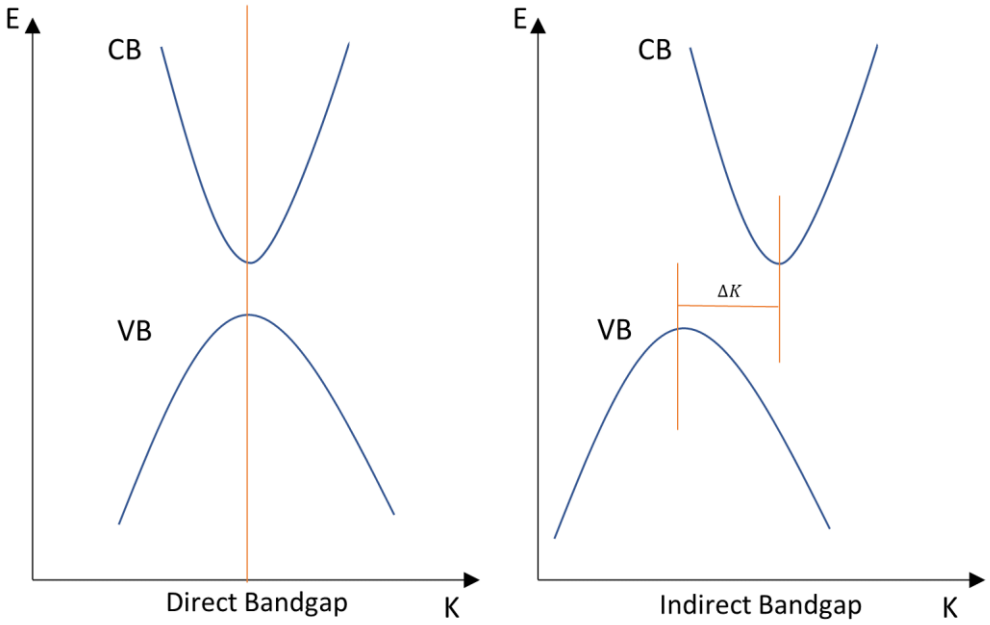

Figure 1.10. The energy-momentum diagram for Direct and Indirect materials.

1.6.2.2 Auger Recombination

Unlike the band-to-band recombination, auger recombination is not a radiative process. This recombination usually involves three particles. Depending on whether it happens on the conduction band or valence band, it will affect two electron and one hole or vice versa. Two electrons (holes) will collide, and as a result, the electron-hole pair will recombine. The resulting excess energy will not be released in the form of a photon as was the case in the aforementioned recombination type but will rather be absorbed by the third particle and cause it to elevate to a higher energy state.

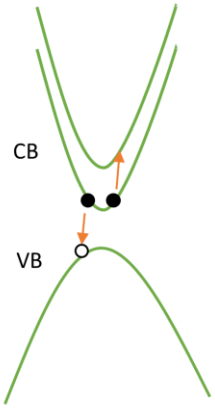

Figure 1.11. Auger recombination.

The auger recombination rate is calculated as the total of electron-electron-hole or hole-hole-electron pair recombination rates[19] :

$$R_{Auger} = R_{eeh} + R_{ehh} = C_n \left(n^2 p + n_{i,eff}^2 n_0\right) + C_p \left(np^2 - n_{i,eff}^2 p_0\right) \quad (1.13)$$

Where C_n and C_p are respectively the n-type and p-type auger coefficients.

The auger lifetime for highly doped semiconductors then can be calculated roughly as:

$$\tau_{Auger,hi} = \frac{1}{(C_n + C_p)\Delta n^2} = \frac{1}{C_a \Delta n^2} \quad (1.14)$$

As it is evident in the eq1.14, The auger lifetime is inversely related to the square of the carrier concentration Δn . Therefore, auger recombination is among the leading causes of lifetime loss in highly doped silicon solar cells.

1.6.2.3 Defect States Recombination

Defect recombination, which is also known as the Shockley-Reed-Hall (SRH) recombination model, occurs when a minority carrier (either an electron or hole) gets entrapped in the trap states located within the bandgap and recombines with a carrier in the valence or conduction band. The carrier typically loses its energy by giving it out as a phonon[20].

The trapped states are either created by impurities such as metals like Fe, Ni, W, or they result from vacancy or misalignment of atoms, which results in some silicon bonds remaining unattached and acting as trapping sites for the free carriers.

Figure 1.12 shows the Auger recombination.

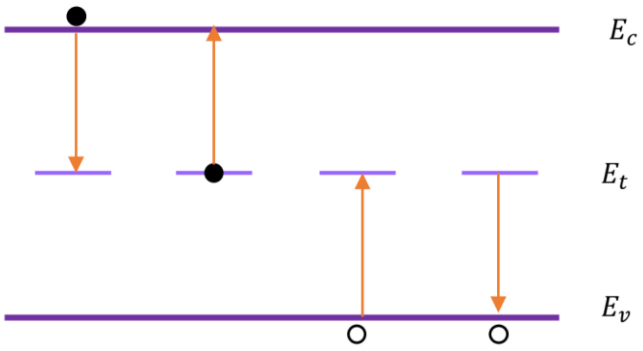

Figure 1.12. The entrapment and emission of carriers according to the SRH model.

Shockley Reed and Hall came up with a model to calculate at what rate the defect recombination will occur with the assumption that only one trap level exists in the bandgap[21][22].

$$U = U_n = U_p = \frac{(np - n_i^2)}{\tau_{p0}\,(n_1 + n_2) + \tau_{n0}(p + p_1)} \tag{1.15}$$

Where U is the total capture rate per unit volume and τ_{n0} and τ_{p0} are:

$$\tau_{n0} = \frac{1}{\nu_{th}\sigma_n N_t} \quad (1.16)$$

$$\tau_{p0} = \frac{1}{\nu_{th}\sigma_p N_t} \quad (1.17)$$

All these recombination mechanisms affect the minority carrier's lifetime severely. Therefore, it is of utmost importance to minimize the defects and impurities in the silicon bulk.

1.6.3 Surface Recombination

The recombination of carriers on the border of the silicon emitter and the additional layers is called surface recombination. Flaws or impurities aid the recombination within or on the surface of the semiconductor. Because the crystal lattice on the solar cell's surface is majorly disrupted, the recombination rate in this area is specifically high. Minority carriers get vastly recombined due to this high recombination rate. These recombination mechanisms are pretty similar to the ones previously discussed except for the fact that, unlike the bulk recombination, where the Recombination-active interface states are in a particular energy level, the surface recombination states are often dispersed continuously over the whole bandgap

In order to avoid this type of recombination, a passivating layer is added on top of the emitter layer.

1.7 Passivation

Passivation is one of the most vital points in manufacturing solar cells. In fact, it's essential for attaining high conversion rates. A significant percentage of the advancement in record-breaking silicon cells has been made feasible by this technology.

There are typically two types of passivation: chemical passivation and electric field-effect passivation.

In the chemical passivation, the focus of the formed passivating layer is to deliberately induce chemical bonds with the recombination trap sites (dangling bonds) to stop the recombination. [23]

In field-effect passivation, the aim is to create an electrical field to repel the minority carriers away from the surface via the use of an electric field present on the surface, and this field is created by the charges existing in the dielectric layer. This field either occurs during the layer deposition process (intrinsic FEP) or is manually produced by the use of ions (extrinsic FEP). one example of this method is the use of specific equipment for electrical discharge (corona) ejection. [24]

Most of the passivation layers used for silicon solar cell passivation utilize both CP and FEP technics for the maximum passivation effect.

Various materials are used in producing an efficient passivation layer for the silicon solar cell.

1.7.1 Silicon Oxide (SiO2)

Silicon oxide does an efficient job of neutralizing the dangling bonds, and since the oxide growth process is relatively easy and implementable, it is one of the commonly known passivation methods for silicon solar cells.

Another advantage is the reduction of potential induced degradation (PID), which happens when the output plummets due to the potential inequality between the PV module and the ground. [25]

The early phosphorus-diffused n^+ emitters were mostly passivated by SiO2 produced at high temperatures. However, in the case of industrial production of solar cells, the high-temperature method is not desirable because of the high cost and the possible physical damages caused by the high temperature.

As in the case of boron-doped p^+ emitters, the SiO_2 layer does not yield the same passivation results as the n-type emitters. Furthermore, p-type emitter solar cells passivated with SiO2 are reported to be very unstable when placed in atmospheric conditions [26]. This can be attributed to the SiO_2's moisture susceptibility, and adding an efficient waterproof coating, such as Si_3N_4, may help slow down the deterioration.

1.7.2 Aluminum Oxide (Al_2O_3)

Aluminum oxide (Al2O3), which is a dielectric material containing negative charges, has been an excellent passivation material for crystalline silicon surfaces.

This passivation layer was first introduced by Jaeger et al. as an efficient passivation method for silicon-based solar cells in the 1980s [27].

However, the first results that showed that this passivation layer could be promising at industrial levels were achieved almost 20 years later [28].

There are different methods of depositing the Al_2O_3 passivation layer. One of the most widely used methods is atomic layer deposition (ALD). It can also be done by the plasma-enhanced chemical vapor deposition (PECVD), reactive sputtering, atmospheric pressure chemical vapor deposition (APCVD), or inductively coupled Plasma (ICP) deposition.

One of the drawbacks of this passivation method is that when it is implemented as this layer, in later high-temperature firing processes, some degradation in this layer can take place. But this drawback is easily preventable by applying hydrogen incorporating layers like SiNx. This layer will alleviate the degradation effects to some degree.

1.7.3 Amorphous Silicon (a-Si:H)

Amorphous heterojunction silicon solar cells Yielding high open-circuit Voltage (Voc) as a results of employing an amorphous layer as passivation are a proof of this layer's passivation capabilities [29]. Surface of HJT solar cells is passivated via the hydrogenation of the states located on the surface. The hydrogen is provided by the amorphous layer. This passivation method is widely used in both p and n-type silicon Heterojunction solar cells, which are comprised of a hydrogenated amorphous silicon (a-Si:H) film on top of crystalline silicon (c-Si). This amorphous layer is deposited at a shallow temperature using the method of plasma-enhanced chemical vapor deposition (PECVD). This method produces good efficiency values in both p and n-type silicon wafers. However, one of the downsides of amorphous layer passivation is its extreme sensitivity to high temperatures. Therefore, the rest of the manufacturing processes need to be done under low temperatures; otherwise, the amorphous layer can undergo some severe degradation.

1.7.4 Silicon Nitride (SiN)

SiN_x produced by PECVD, on top of being an anti-reflection coating (ARC), is also frequently employed as a passivating layer for industrial silicon solar cells. Si_3N_4 is the most widely recognized type of silicon nitride which is widely used in micro-level fabrications, and it is commonly produced using either LPCVD or PECVD based on one of the reactions listed below:

$$3SiH_4(g) + 4NH_3(g) \rightarrow Si_3N_4(S) + 12H_2(g) \quad (1.19)$$

$$3SiCl_4(g) + 4NH_3(g) \rightarrow Si_3N_4(s) + 12HCl(g) \quad (1.20)$$

$$3SiCl_2H_2(g) + 4NH_3(g) \rightarrow Si_3N_4(S) + 6HCl(g) + 6H_2(g) \quad (1.21)$$

PECVD SiN can effectively passivate both p-type and n-type silicon surfaces with low and medium doping levels. although its passivating effects on p+ boron doped substrates have observed to be more challenging, It works well on highly doped n+ diffused layers.

CHAPTER 2

METHODOLOGY

2.1 Working Mechanism of Fabrication Systems

In this section, all the methods and devices used in the fabrication process of experiment samples are explained in detail.

2.1.1 Forming the Boron Emitter Layer Using the PECVD Method

There are various ways of introducing an element into a substrate, such as Ion implantation, spin-on dopant (SOD), and diffusion using chemical vapor deposition (CVD). The CVD method can be further branched out into different methods based on what kind of techniques are used to initiate the reactions. A few of the examples are APCVD (atmospheric pressure), LPCVD (low-pressure CVD), HDPCVD (high-density plasma CVD), and PECVD (plasma-enhanced CVD)[30].

In ion implantation, the surface is bombarded with high-energy dopant ions that penetrate the substrate and occupy the vacancies in the crystal lattice. Ion implantation allows decent control and is perfect for doping a specific area within the substrate. The ion implantation takes place under relatively low temperatures. However, it causes substantial crystal destruction, necessitating annealing to repair the crystal and activate the impurities inserted, which requires exposing the samples to high temperatures and will increase the costs of the procedures. Because of these factors, ion implantation is a sensitive and expensive procedure.

In Spin-on dopant method, a solution containing the dopant particles is dispersed into the substrate using Spin-on coating; this procedure is followed by rapid thermal annealing (RTA) procedure because an annealing step is required to diffuse the

dopant into the substrate. This processing method offers several benefits, including cost-effectiveness, adaptability to industrial manufacturing, and operation under normal atmospheric conditions. Nevertheless, it does not yield efficient results for the fabrication of the boron emitter layer.

The CVD system consists of a furnace connected from one end to the gas sources and from the other end it is connected to the exhaust line, where gaseous byproducts exit the furnace. The substrate inside the furnace is heated up to temperatures ranging from 600 to around 1000°C. The reactant gases enter the chamber and react with each other and the sample substrate, these sets of reactions result in the formation of a solid layer on the substrate and other byproducts in the form of gas which will eventually exit the chamber. This set of actions is depicted in Figure 2.1.

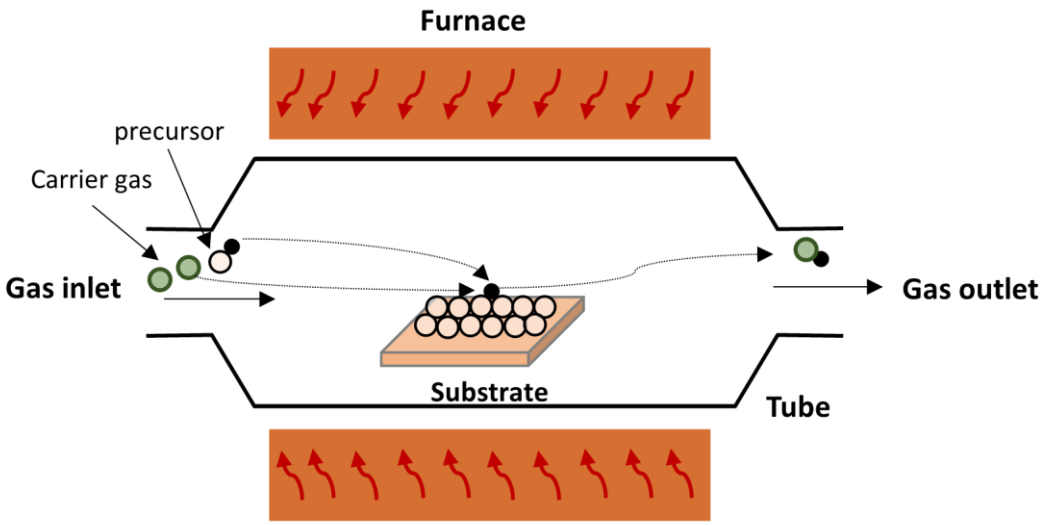

Figure 2.1. Cross-section of a CVD furnace.

One advantage of this system is that the deposition can reach every part of the samples, including the areas that are impossible to reach with other coating methods. Since it can be processed in batches, it is highly suitable for mass production and industrial purposes. However, the process temperatures are very high, making this process undesirable since the high heat can severely damage the samples, rendering them unusable.

Plasma-enhanced chemical vapor deposition (PECVD) mechanism is one of the variants of the conventional CVD method and it is one of the most efficient ways of diffusing a dopant into the desired substrate and it is also utilized in deposition of various layers during this thesis work.

In PECVD, thin films of various materials can be deposited on substrates at lower temperatures than standard Chemical Vapor Deposition (CVD). It is used for the deposition of multiple layers such as silicon dioxide (SiO_2), silicon nitride (Si_3N_4), silicon oxynitride ($Si_2N_2O_2$), BSG, PSG, and amorphous silicon (α-Si).

Unlike the conventional CVD method, where only thermal energy is used, the thin films are deposited using plasma energy. Direct current or Radiofrequency is commonly used to generate plasma by energizing the reactant gases.

The electrodes located on the two ends, one grounded and one energized, supply plasma energy after the reactive gases are injected into the reactor. As a result, the gas molecules break down inside the plasma. The various chemical species produced react with one another and the interface substrate. The substrate is around 300° C which is a lot lower than the temperature for the CVD system, making PECVD a better alternative when working with more delicate samples. The SEMCO LYDOPTM furnace system is used at the facilities of the GÜNAM research center to dope boron and phosphorus layer.

Figure 2.2. SEMCO LYDOPTM furnace (PECVD system) in GÜNAM research center.

PECVD furnace is widely used in deposition of Boron emitter layer which is also the focus of this work. The two most used sources for boron are $BOCl_3$ and BBr_3. Other supplementary sources of gases such as O_2 and N_2 are also incorporated in the diffusion process to help with the reactions and doping uniformity.

The reactions that occur during the diffusion process under vacuum conditions are as follows :

$$4BCl_3 + 3O_2 \rightarrow 2B_2O_3 + 6Cl_2 \qquad (2.1)$$

The Boron oxide, together with the SiO_2 that is formed on the surface of the silicon samples will be creating a layer named Borosilicate glass (BSG) on the surface of samples. it will then go on to react with silicon which results in the samples being doped with boron:

$$2B_2O_3 + 3Si \rightarrow 4B + 3SiO_2 \qquad (2.2)$$

To better understand how the silicon is doped, it is helpful to understand what happens in the crystal lattice when an element approaches it.

2.1.1.1 Doping a Crystal Lattice

Doping is generally known as a form of defect. When an impurity atom different from the host element occupies a state within the crystal lattice, doping takes place. On average, crystals can withstand a few impurity atoms per million initial substrate atoms. There are a few possibilities that can occur. When a dopant atom approaches the structure, the dopant can either occupy the place of a host atom within the structure, called substitutional doping. In this case, the impurity either occupies an already available vacancy, or replaces a host atom by pushing it out.

It can also take an interstitial position between the atoms that is not a part of the lattice (interstitial doping). The first method is more desired since in this method, the atoms are already electrically active. In the second method, for the doped atoms to to contribute to the electrical characteristics of the samples actively, they must be activated by exposure to high temperatures.

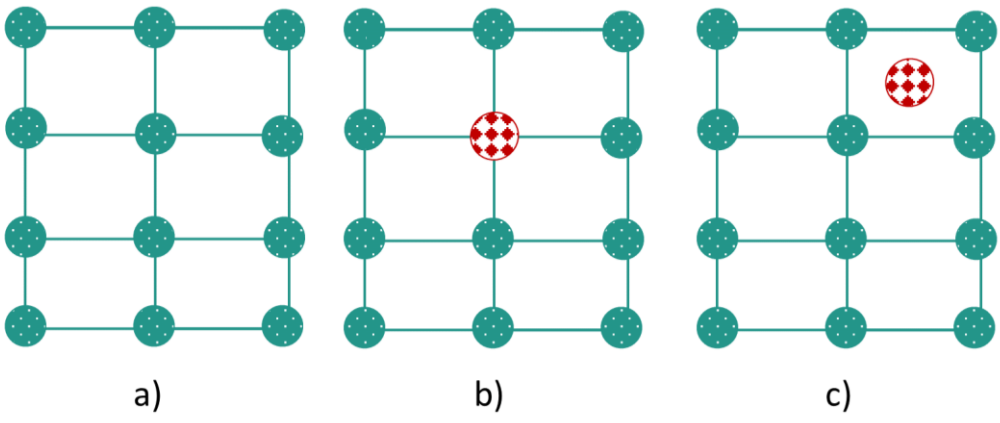

Figure 2.3. a) Intrinsic Lattice Structure b) Substitutional Doping c) Interstitial Doping.

2.1.2 Atomic Layer Deposition (ALD)

Atomic Layer Deposition is another method of depositing thin layers similar to the chemical vapor deposition (CVD) method. This thin film deposition method is utilized where there is need for an atomic level of control in the layer thickness. Its difference from the CVD method is that the precursor material pulses are injected into the furnace sequentially. This gives an immense level of control in layer deposition. ALD works in cycles that include four stages:

1) introducing the first precursor gas.

2) cleansing or purging the remaining gas and side products of the reaction from the furnace.

3) releasing the second reactant gas, typically oxidants or reagents.

4) purging the reaction byproducts from the furnace.

This cycle of four stages will be implemented until the desired layer thickness is achieved.

This method is used in the formation of the Al_2O_3 passivation layer. Usually, extremely thin layers of Al_2O_3 is required (nanometer scale) during the fabrication of crystalline silicon solar cells, which makes the ALD a suitable deposition method.

The primary reaction taking place during Al_2O_3 passivation layer formation is :

$$2\,Al(CH_3)_3 + 3\,H_2O \rightarrow Al_2O_3 + 6\,CH_4 \qquad (2.3)$$

The Figure 2.4 depicts the 4 cycles of ALD for the Alumina deposition.

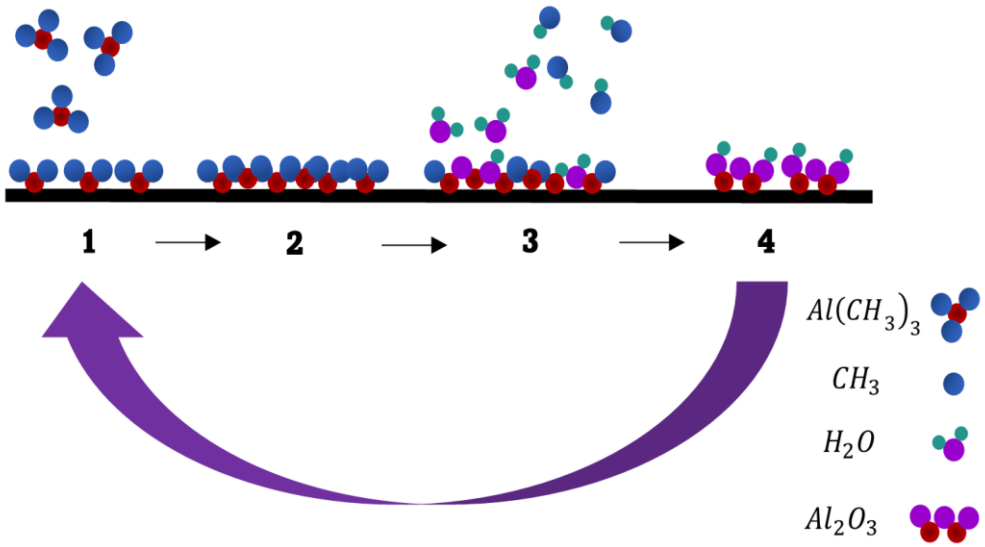

Figure 2.4. Cycle of Al_2O_3 layer deposition in the ALD device using Trimethylaluminium and H_2O as reactant gases.

After each precursor pulse, the furnace is constantly cleansed with a frequently used gas source such as nitrogen, which removes all reaction byproducts, excluding those that are chemically absorbed on the substrate. This action is named purging. As a result, film development occurs through a series of surface and gas interactions, allowing for self-limiting and self-controlled development. Because of the auto-controlled layer formation, the developed film thickness can be controlled in angstrom level precision by the number of cycles.

Another significant benefit of self-controlled ALD growth is that even intricately shaped structures can be evenly covered. This method is mainly executed under lower temperatures, making it ideal when dealing with heat-sensitive materials.

It is important to note that despite the many advantages of ALD processes, layer deposition might not always be executed flawlessly. However, Most ALD procedures result in the deposition of a sub-monolayer after each cycle, primarily due to nonbonding interaction between the precursor materials. This phenomenon results in blockage of the active sites. Furthermore, irregular crystallization sites or

diffusion might lead to the formation of islands or nanoparticles rather than a uniform sheet layer.[31]

The ALD system used throughout the experiments that took place in this work is shown in figure 1.4. The system consists of two parts, gas supply unit (GSU) and process development tool (PDT).

Figure 2.5. ALD system in GÜNAM research center. (a) is the GSU and (b) is the PDT.

2.1.3 Metallization with Screen Printing

Forming a mesh of narrow metal lines on both sides of bifacial crystalline silicon solar cells is one of the most critical manufacturing processes. Screen printing is one of the oldest and most frequently used industrial solar cell production methods and is very straightforward to implement. As a starter, a printing mask must be placed over the silicon wafer at a specific distance known as the Snap-off distance. This mask is a detailed mesh structure of the desired design of fingers and busbars fitted into a frame. This allows the metal paste to form the desired shape with ease. The paste is a conductive substance made up of metal particles such as Silver and Aluminum.

The paste is evenly distributed on the wafer with the help of a spreading tool (squeegee). Temperature, applied pressure, and pace must remain constant throughout the process to achieve uniformity.

Figure 2.6. Screen printer system in GÜNAM research center.

The sample must be adequately dried after the process by placing them in a drying furnace; the final step is firing the samples at high temperatures to allow the printed metal to adhere to the sample and build contact with it. The backside of samples is either fully covered with metal paste or in the case of a bifacial cell, is screen-printed like the front side. However, the metal fingers for the backside do not require to be as fine as the front side.

The metal printing can be implemented multiple times after each drying process. This enables us to control the finger thickness with micron-level precision.

Figure 2.7. The drying oven used in the GÜNAM research center.

Figure 2.8. The Firing Furnace used in GÜNAM research center.

2.2 CHARACTERIZATION METHODS AND SYSTEMS

Various measurement methods and devices have been utilized throughout this work to characterize and optimize each of the implemented fabrication steps in sample production.

2.2.1 TLM (Transfer Length Method)

Contact resistance is measured via different methods and sample structures. Some examples are TLM, circular TLM (CTLM), and Cox and Strack Method (CSM). The Transfer length method (TLM), also known as the Transmission line method, is an extensively used method utilized in this work. Through this measurement method, values such as emitter sheet resistance (R_{sh}), contact resistance (R_c), and contact resistivity (ρ_c) can be obtained.

The first requirement for using this measurement method is that the layer underneath the metal fingers must be thinner than the minimum linear contact distance. Since this requirement is fulfilled between the solar cell emitter and the metal fingers, we will be using the TLM for contact resistance measurements.

The conventional TLM structure used for this measurement method consists of a series of string-shaped metal fingers placed parallel on a thin layer. The distance between the fingers slightly increases with each sequence[32].

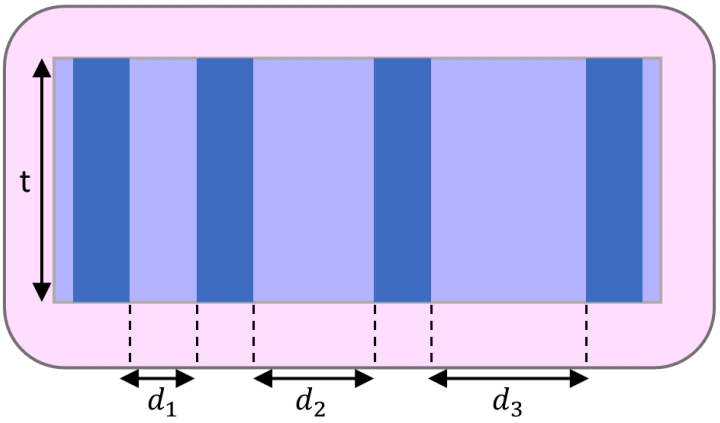

Figure 2.9. the conventional TLM measurement structure

$$R_{Sum} = 2R_m + 2R_c + R_{se} \quad (2.4)$$

Where R_{Sum} is the sum of all types of resistances present in the TLM structure, R_m is metal contact resistance, R_c is the contact resistance between the metal and semiconductor and R_{se} is the semiconductor material resistance.

In this calculation, the metal finger's contact resistivity is assumed to be zero:

$$R_m = 0 \tag{2.5}$$

$$R_{sem} = R_S \frac{d}{t} \tag{2.6}$$

Where R_S stands for the series resistance, d is the distance between 2 metal stipes and t is the width of the metal stripe.

By replacing R_{sem} in Eq 2.4 with Eq 2.6, we will have:

$$R_{Sum} = \frac{R_S}{t} d + 2R_C \tag{2.7}$$

By plotting the total resistance versus finger distance graph, it is possible to extract the contact resistance and the sheet resistance, respectively, as the graph line's intersection and the y axis and the slope of the graph line.

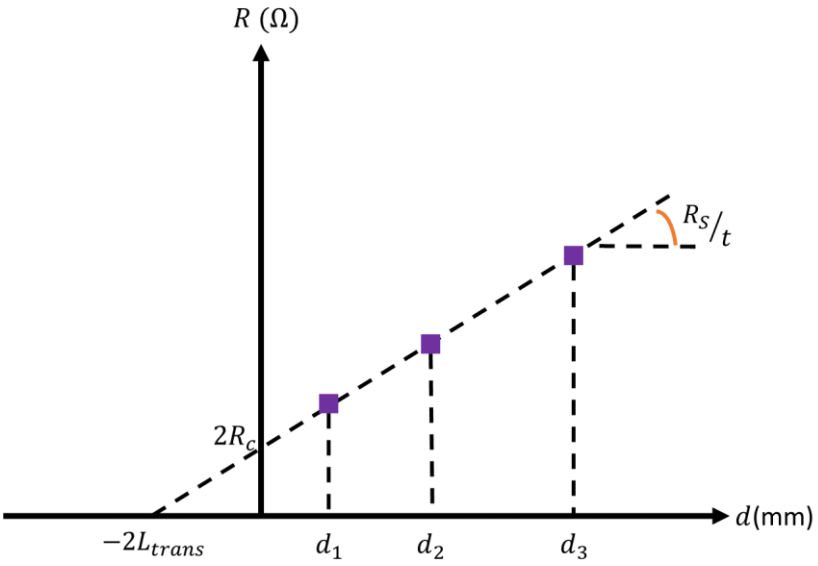

Figure 2 10. The resistivity-finger distance graph.

Since contact resistance is dependent on the area, it is more efficient to use resistivity instead. In order to calculate it through the same method used above, it is required first to introduce a new term called transfer length (L_{trans}). the current flows laterally from one metal finger to the next. However, this current flow is not evenly distributed in the finger; it accumulates at the starting point of the finger. This phenomenon is called "current crowding." It has been seen that the current flow plummets exponentially as we get further away. This is because the carriers keep getting absorbed by the metal contact. In fact, it becomes almost zero at the length L_T.

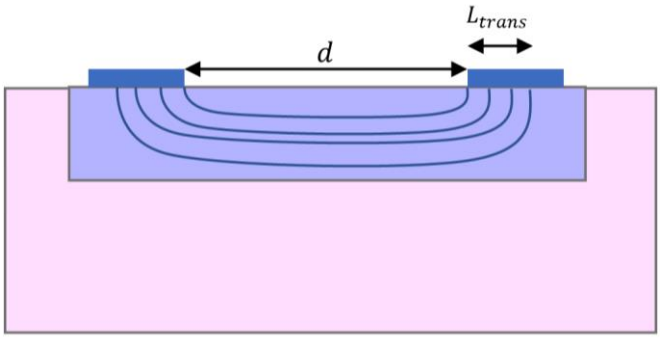

Figure 2.11. Transfer length in TLM structure.

$$L_{trans} = \sqrt{\frac{\rho_c}{R_S}} \tag{2.8}$$

Where ρ_c is the contact resistivity. Now the contact resistivity can be calculated using the effective area:

$$R_C = \frac{\rho_c}{L_{trans} t} = \frac{L_{trans} R_S}{t} \tag{2.9}$$

By replacing R_c in Eq 2.7 with Eq 2.9, we will have:

$$R_{Sum} = \frac{R_S}{t} L + 2\frac{L_{trans} R_S}{t} \tag{2.10}$$

$$R_{Sum} = \frac{R_S}{t} (\mathrm{d} + 2L_{trans}) \tag{2.11}$$

To measure our TLM samples, full wafers are cut into 1 cm long stripes and are measured with the PVTOOLS system (shown in figure 2.13.). This system utilizes automatic probes to measure the contact resistivity between two fingers.

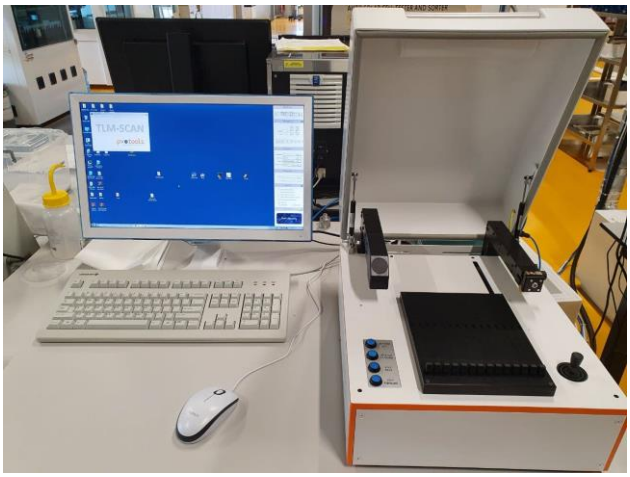

Figure 2.12. PVTOOLS System in GÜNAM research center.

2.2.2 Four Point Probe (4PP)

This method is used to measure the emitter and bulk sheet resistance. The structure is composed of 4 probes placed linearly on the sample. The outer probes measure and induce the current, and the inner probes measure the voltage. The p-n junction prohibits the current from flowing into the bulk, keeping it constrained in the emitter region [1].

$$\rho_{sq} = \frac{\pi}{\ln(2)} \frac{V}{I} \tag{2.12}$$

Where:

$$\frac{\pi}{\ln(2)} = 4.532 \tag{2.13}$$

ρ_{sq} is the sheet resistivity, and V and I are the measured voltage and current.

The thickness (t) should also be included in the calculation when measuring the bulk sheet resistance. Here, the sample is presumed to be thinner than half the distance between the probes. Therefore, the sheet resistance can be calculated with Eq 2.14:

$$\rho = \frac{\pi}{\ln(2)}\left(\frac{V}{I}\right)t = 4.532(\frac{V}{I})t \quad (2.14)$$

Figure 2.13. Four-point probe device used in GÜNAM research center.

2.2.3 Electrochemical Capacitance-Voltage (ECV) Device

This tool is used to obtain the doping profile of the emitter to analyze how the doping concentration changes as we go deeper into the emitter.

However, this method is only used for active dopants, and it cannot be used for inactive dopants measurement. The chemical used as an electrolyte must have the minimum chemical etch possible. Optimally, if there is no current, introducing the electrolyte to the wafer should result in zero etching.

When the emitter is p-type as it is in this work, a forward current between the electrode and the sample surface will be applied to force the majority positive carriers to flow to the semiconductor surface, recombining with 4-valence electrons of the silicon atom and removing the atom from the surface through the current. As a result, the semiconductor can be etched with decent control.

In order to measure the carrier concentration, the capacitance is constantly measured as the applied voltage changes since an AC current is applied. The metal electrode's contact with the semiconductor results in a Schottky barrier formation because the surface charges flow into the metal electrode and deplete the surface. This depleted barrier width varies with the change in the applied voltage change. The capacitance also simultaneously undergoes a transformation.

Therefore, the carrier density can be measured by utilizing the Mott Schottky equation [1]:

$$\frac{1}{C^2} = \frac{-2}{e\varepsilon_0\varepsilon_R A^2 N} \cdot (V - V_{fb}) \tag{2.15}$$

$$N = \frac{-2}{e\varepsilon_0\varepsilon_R A^2 . \frac{d(1/C^2)}{dV}} \tag{2.16}$$

Where C is the measured capacitance, e is the Electron charge and is approximately equal to 1.6×10^{-19} C, ε_0 is Vacuum permittivity and is approximately equal to 8.85×10^{-12} C/Vm, ε_R is the relative permittivity of the semiconducting material, A is the measurement area, N is the carrier concentration, V is the applied voltage and V_{fb} is the flat-band potential.

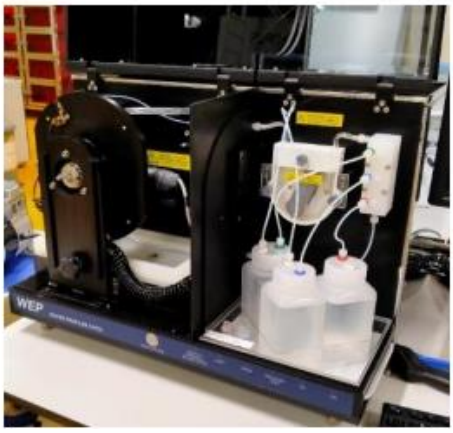

Figure 2.14. The ECV system in GÜNAM research center.

2.2.4 Photoluminescence Inspection (PLI)

Photoluminescence Inspection has been utilized to detect all the defects and inhomogeneity on the sample surface by producing a clear image. Figure 2.15 shows the generation of a Photoluminescence signal.

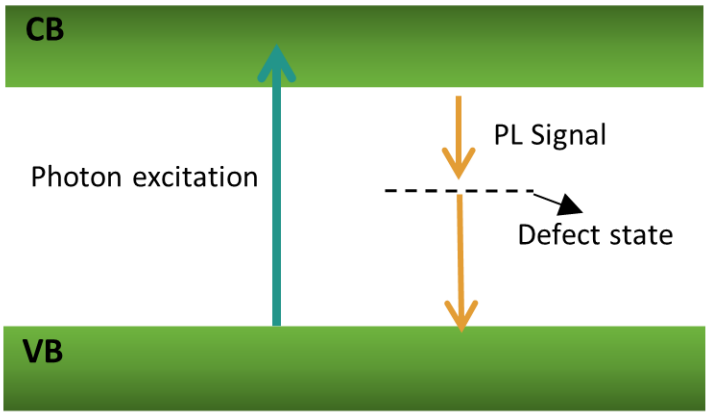

Figure 2.15. Photoluminescence Signal generation.

It also yields important values such as carrier lifetime and implied Voc mapping of the surface. As mentioned before, various recombination types can occur in a solar cell when exposed to a light source. The radiative recombination here is a key factor in the measurement mechanism of PL. By subjecting the sample to light and then detecting the photons radiated back PL is able to spot the defects and problems within the sample.

The image in Figure 2.16 shows the Photoluminescence inspection system used in this work.

Figure 2.16. Photoluminescence Inspection System in GÜNAM research center.

2.2.5 I-V Measurement

To investigate some important solar cell values, such as the I-V curve from which the V_{oc} and I_{SC} values are derived, the efficiency, the fill factor, and the series and sheet resistance, the I-V measurement device is used. This device works by replicating the AM 1.5 conditions of the sun.

The device can be utilized in both dark and illuminated conditions. The first condition gives us an understanding of how the solar cell would behave as a diode. The latter provides insight into the cell's behavior as an electricity-producing active solar cell.

Figure 2.17. The QuickSun 120CA-XL flash solar simulator system used for I-V measurements in the GÜNAM research center.

2.2.6 Lifetime Test Measurement

When a solar cell is exposed to sunlight, the photons with an energy higher than the silicon’s bandgap will get absorbed by carriers exciting them to a higher state. The amount of time they have before recombining is called recombination lifetime. It is possible to measure the lifetime under both transient and quasi-steady-state (QSS) conditions. The light exposure duration is concise in the transient mode, so it’s more suitable for measuring samples with a high expected lifetime. however, in QSS mode, the light intensity is reduced slowly. This method is perfect for testing the quality of doped samples, specifically, the samples with lesser expected lifetime.

Also, it is possible to measure characteristics other than sample lifetimes, such as average sheet resistance, saturation current density (J_0), and 1-sun implied open-circuit voltage (imp V_{oc}) [33]. This measurement provides a practical estimated lifetime for the measured sample considering the effect of all the recombination factors introduced in section 1.6.2.

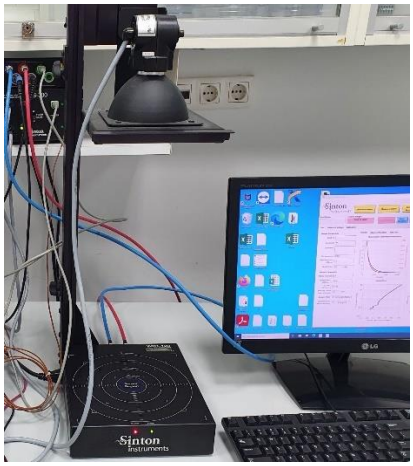

Figure 2.18. Sinton W120 lifetime tester device used for lifetime measurement in GÜNAM research center.

CHAPTER 3

EXPERIMENTAL DETAILS

The primary purpose of this experimental work is to optimize the boron emitter layer utilized in the fabrication of n-type bifacial solar cells. Therefore, two sets of experiments were designed to achieve an optimized recipe for the emitter layer. Finally, Bifacial Solar cell Structures were fabricated employing the previously optimized layers and parameters.

3.1 Wafer texturing and cleaning

1-5 Ω.cm n-type and 1-3 Ω.cm p-type wafers with an area of $156.75 \times 156.75\ mm^2$ and a thickness of 170 μm was utilized in this experimental set.

Firstly, the samples were textured and cleaned employing the recipes previously optimized at the GÜNAM research center. Wafers were textured using a mixture of Potassium hydroxide (KOH) and Alka-Tex diluted with distilled water. Texturing took place at around 80° C. Afterwards, RCA-1 and RCA-2 cleaning recipes were used to remove any residues left after the texturing process. These cleaning steps were repeated between the fabrication steps to remove any pollution and contaminant that might attach to the samples. RCA-1 cleaning recipe consists of chemicals such as Ammonium Hydroxide (NH4OH), Hydrogen Peroxide (H2O2), and DI water. RCA-2 cleaning recipe contains Hydrogen Peroxide (H2O2), Hydrochloric Acid (HCl), and DI water.

Both these cleaning steps were taken place at approximately 70° C temperature. During RCA-1, bigger particles attached to the wafers are removed. The Ammonium Hydroxide reacts with the surface and etches the oxide layer underneath the pollutants. the Hydrogen Peroxide creates a new oxide layer to help protect the

surface from getting over-etched. The RCA-1 cleaning recipe might cause other smaller metal contaminants to aggregate on the sample surface. Thus, the second cleaning process should follow the first step to remove these metal pollutants from the surface.

3.2 Boron doping

The boron doping process for the samples was done using the PECVD furnace. The deposition step took place under vacuum conditions with a pressure of 400 mbar, BCl_3 gas was used as the precursor and N_2 as the carrier gas. The diffusion process took about 15 minutes. Then a dive in step with O_2 and N_2 as the supplementary gases was carried out for around 30 minutes to complete the doping process. The temperature at which the doing process was taken place was around 937℃. The ratio of the precursor gases used during the doping is shown in Table 3.1.

Table 3.1 Gas ratios used in PECVD Boron doping.

Gas type	*Gas ratio*
Boron trichloride (BCl_3)	50
Carrier Nitrogen (N_2)	1500
Oxygen (O_2)	800
Nitrogen (N_2)	1500

Both sides of the samples were uniformly doped with a boron-rich layer (BRL) filled with inactive boron dopants covering the surface. This BRL layer is tricky to remove since the silicon layer is not easily etched. Therefore, an oxidation step is required to oxidize this boron-rich layer to make the etching possible.

3.3 BRL removal

The samples were oxidized to remove the boron-rich silicon layer successfully. Three different recipes for oxidation have been utilized for this experimental set. Two thermal oxidation recipes and a low-temperature chemical etching.

For the first oxidation recipe, the samples were oxidated using a ratio of 2000 Sccm oxide with a temperature of 850 ℃ . for the second recipe, 600 Sccm of O_2 and 1000 Sccm of H_2 was used for oxidizing the samples at 850 ℃. The details of the two thermal oxidation recipes are shown in Table 3.2.

Table 3.2 Comparison of Thermal Oxidation recipes.

Recipe name	O_2	H_2	*Temperature (℃)*
Pass3	2000	-	850 ℃
LTOnew	600	1000	850 ℃

The chemical solution used in the third and last recipe consists of 6 liters of distilled water, 0.8 liters of hydrochloric acid (HCl), and 0.8 liters of hydrogen peroxide (H_2O_2). the oxidation process was done at a relatively low temperature of 85℃. The samples were dipped in the solution for 15 minutes. All three oxidation recipe samples were later dipped in a solution of 10 percent HF for one minute to remove the oxidized boron-doped silicon surface, also known as borosilicate glass (BSG). The BRL layer removal is a vital step because the existence of the BRL layer can cause the surface recombination to increase radically. Also, Due to the misaligned refractive index of BRL and SiO_2/SiN_x , for samples passivated with SiO_2/SiN_x Stack layer, the presence of BRL can reduce the minority carrier lifetime by

weakening the anti-reflection effect. Various research has indicated that the composition of Si-B in BRL is commonly suggested to be SiB_6 which can be oxidized to B_2O_3 easily in the oxidizing atmosphere.

To investigate the uniformity of boron doping and etching, sheet resistance values for the samples were measured using the four-point probe. The p-type samples were also contemplated in this doping examination to investigate the quality of the boron doping as a back surface field (BSF) layer.

In order to ensure the doping is uniformly done, R_{sh} mapping was carried out by taking the measurements on nine various sides of the samples, as marked in Figure 3.1. the measurements are done from left to right and up to down. The upper left side of each sample is marked with a laser marker.

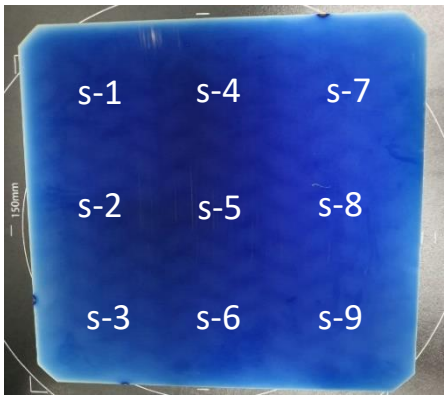

Figure 3.1 R_{sh} measurements were taken from the marked areas shown in this image.

The Boron dopant concentration of the samples was also measured using the electrochemical capacitance-voltage (ECV) system.

3.4 Emitter Passivation and ARC layer deposition

Both $Al_2O_3/\ SiN_x$ and $SiO_2/\ SiN_x$ Stack passivation layers were tested on the lifetime samples to investigate the passivating properties of these Stack layers. The samples passivated with Al_2O_3 were layered with a 2 nm and 5nm thick alumina layer by doing 15 and 37 Passivation ALD cycles. the atomic layer deposition (ALD) was used to deposit the Al_2O_3 passivation layer. after Al_2O_3 deposition, samples were annealed at 425 ° C for 30 minutes to activate the passivation. Then an ARC layer was deposited using the PECVD system.

the samples passivated with $SiO_2/\ SiN_x$ stack layer were first oxidized with the dry oxidation method in the PECVD furnace at 850° C to passivate the surface. As for the ARC layer, two different SiN_x Recipes were compared to achieve the best result. Photoluminescence (PL), implied $V_{oc,}$ and minority carrier lifetime measurements were carried out. The details of the two SiN_x recipes are stated in Table 3.3.

Table 3.3 Comparison of SiN_x recipes.

	Sirich	Sirich3
Chemical composition	SiH4:135, NH3:1088	SiH4:80, NH3:1222
Temperature	380°C	380°C
power	325 Watt	325 Watt
Reflective index	1.92	1.89

The passivated samples were fired at 910°C before moving to the metallization step. Another set of photoluminescence and implied V_{oc} measurements were carried out to observe the effects of firing. Also, one ECV sample from each oxidation recipe was fired to monitor the firing effect on carrier concentration. Figure 3.2 depicts the lifetime sample's process flow and a cross-section of each fabrication step.

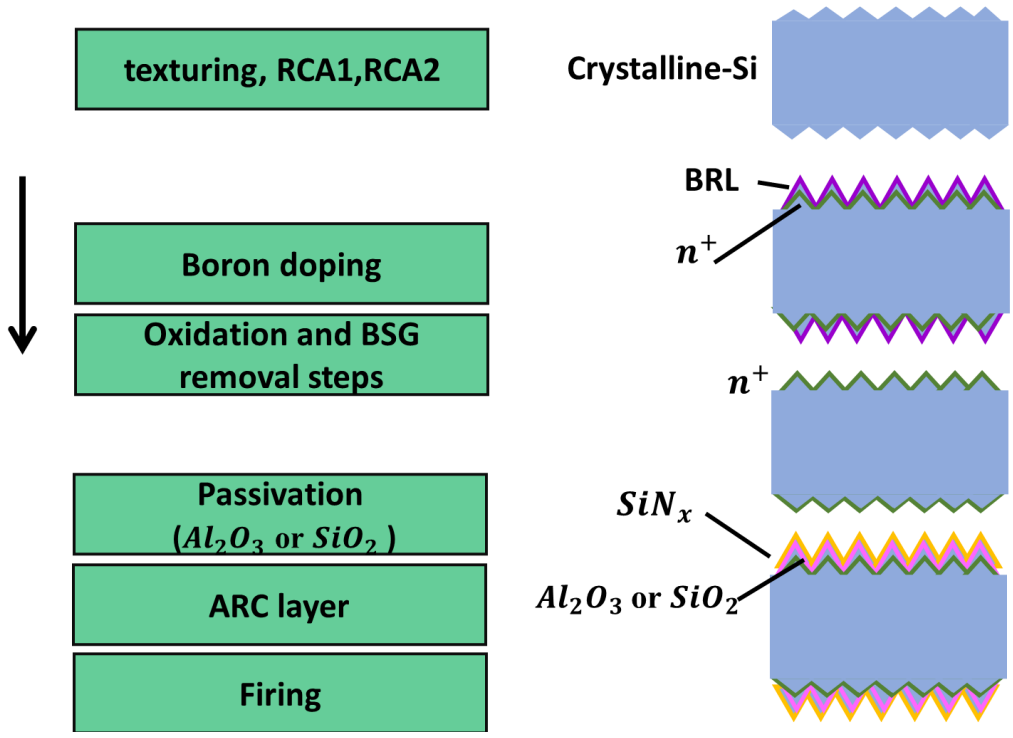

Figure 3.2. Flowchart and Cross-section of lifetime sample's experimental steps

3.5 Metallization And TLM Measurements

After finishing the passivation and firing steps and obtaining the required characterization measurements, The lifetime samples were converted to TLM samples. Fingers and busbars with an H-grid pattern were printed on one side of the samples with the screen printing method utilizing a pre-designed mask for the design and the Ag/Al paste. Figure 3.3 shows a microscopic image of screen-printed fingers.

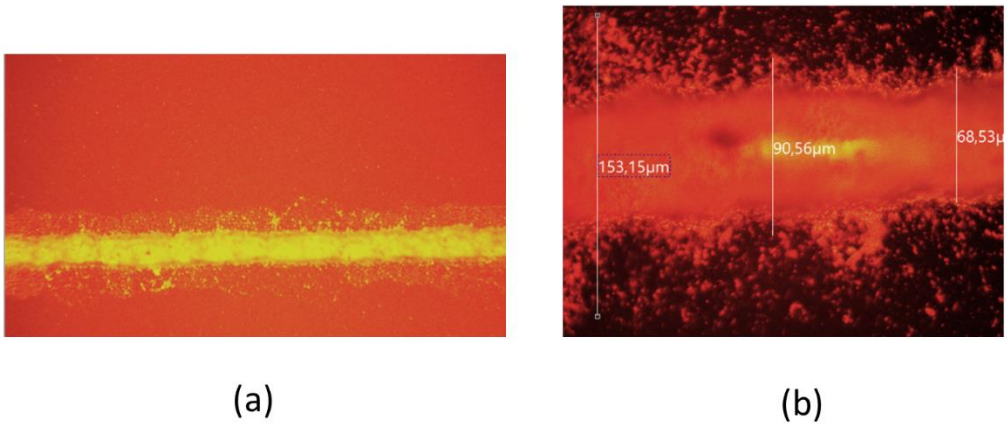

Figure 3.3. Microscopic image of screen-printed fingers at (a) 10x and (b) 40x magnification.

After printing the samples with metal grids, they were dried using the drying furnace. Dried screen printed samples were then cut into three using the laser cutting device to test different firing temperatures. The belt speed for the firing furnace was kept constant at 500 cm/min. The samples were fired at 850°, 875°, and 900° C to investigate the effect of the temperature alteration on junction formation and contact resistivity of samples. TLM measurement method was used to calculate the contact resistivity of the samples. Fired samples were cut into one centimeter wide stripes with the laser to prepare the samples for the measurement. The cross-section of TLM samples is shown in Figure 3.4.

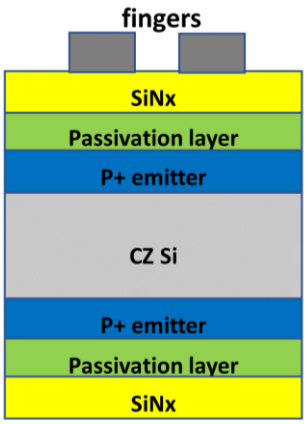

Figure 3.4. The cross-section of TLM samples.

3.6 Second Optimization Test

In this set of experiments, a different wet chemical oxidation recipe was optimized. Also, a low-temperature dry oxidation recipe was optimized for the thermal oxidation process.

1-5 Ω.cm, n-type, Cz wafers with an area of 156. 75 ×156.75 mm^2 and a thickness of 170 μm were utilized in this experimental step. Samples were textured and cleaned with the methods discussed in the previous section. After the texturing and cleaning steps, samples were doped with boron in the PECVD system with the recipe optimized in the GÜNAM research center. This step was identical to the previous set. To optimize the chemical oxidation recipe, two full-size samples were cut into 5.2 x 5.2 cm^2 pseudo-square samples with the help of a laser cutting device. Figure 3.5 shows an example of a chemical oxidation sample.

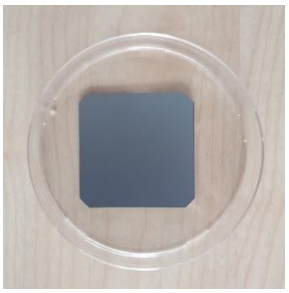

Figure 3.5. Image of sample cut for the oxidation recipe optimization.

A mixture of Nitric acid (HNO3), Acetic acid (CH3COOH), and Hydrofluoric acid (HF) were used as the chemical oxidation solution. The ratio for each chemical component is shown in Table 3.4 below:

Table 3.4 Chemical ratio of the chemical oxidation recipe.

Chemicals	*ratio*
HNO3	100
CH3COOH	100
HF	1

The samples were etched for durations of 2, 3, 4, and 5 minutes to assess the oxidizing and etching properties of the chemical solution. The carrier concentration of oxidized samples was measured with the ECV system.

The R_{sh} values were measured on both sides of the samples using the 4PP device. The lifetime and implied Voc were obtained using the Sinton device.

to use this chemical oxidation recipe on a bigger scale for the oxidation of whole wafers in batches and to reduce the chemical waste and overall cost of the procedure, the chemical oxidation recipe was diluted. The diluted ratio of the chemical compounds is shown in Table 3.5.

Table 3.5 Diluted chemical ratio of the chemical oxidation recipe.

Chemicals	Ratio
HNO3	90
CH3COOH	90
HF	20
H_2O	800

Oxidation test samples were dipped in the diluted solution for durations of 10 and 22 minutes. The doping profile of the diluted chemical oxidation recipe samples was then measured with ECV. The lifetime and implied V_{oc} values of the diluted chemical oxidation recipe were also measured.

After optimizing the chemical ratio and evaluating the suitable etching duration for samples, the lifetime samples were prepared for oxidation.

The lifetime samples were divided into two sets; (set-1) were chemically oxidated and etched using the diluted chemical oxidation recipe. After reviewing the characterization results of diluted oxidation samples, it was assessed that a duration of 16 minutes would suffice to etch and oxidize the samples chemically without causing them any harm.

The set-2 samples were oxidized in the PECVD furnace with the dry oxidation method using a ratio of 2000 Sccm oxide (O_2) with a temperature of 650°C. One of the small-size samples was also oxidized alongside the batch. The developed BSG layer was etched away by submerging the samples in a 10% HF solution. One small unoxidized sample was also etched in HF for later comparison. ECV measurements of the unoxidized and thermally oxidized samples were measured to obtain a doping profile.

Oxidized samples were then cleaned with the RCA method. The lifetime values of the samples were measured using the Sinton system. After the doping and oxidation steps, cleaned samples were passivated with an Al_2O_3/SiN_x stack layer. 2nm thick

Al_2O_3 layer was deposited using the ALD device using 15 deposition cycles. The samples were then annealed for 30 minutes with a temperature of 425°the. the SiN_x ARC layer was deposited using the PECVD system. Two recipes were used for the SiN_x layer. "SiN_1" with a reflective index of 1.96 and “new08” with a reflective index of 1.73. the Al_2O_3/SiN_1 stack layer was named pass4, and the $Al_2O_3/new08$ stack layer was named pass5.

Passivated samples were fired at three different temperatures of 850°, 880°, and 910°C. Because it is an unavoidable step during metallization in order to make certain that the metal-semiconductor contact will be formed successfully. To assess the impact of firing on samples, the lifetime and implied V_{oc} measurements were carried out.

3.7 TLM samples

After the measurements for passivated samples were obtained, the samples were screen printed on one side with H-grid fingers and busbars using an Ag/Al metal paste. After printing the samples with metal grids, they were dried using the drying furnace. The dried TLM samples were then cut into two sections using the laser cutting device. The samples were fired at two different temperatures (880° and 900° C) to investigate the effect of temperature alteration on the contact formation and contact resistivity of samples during the firing process. TLM measurement method was used to calculate the contact resistivity of the samples. To prepare the samples for the TLM measurement, fired samples were cut into one-centimeter-wide stripes with the laser device.

3.8 Bifacial Cell

As previously stated, this study aims to improve the minority carrier lifetime in the emitter layer of crystalline wafers to manufacture an efficient bifacial solar cell. To finalize the optimization of the emitter layer and test the reproducibility of the

obtained optimizations, a set of n-type bifacial solar cells were produced. 1-5 Ω.cm wafers with an area of 156.75 ×156.75 mm^2 and a thickness of 170 μm was used to produce Bifacial cells. The previous sections provide a detailed description of the processes utilized in the fabrication of the cells. The wafers were textured and cleaned before the doping procedures took place. Unlike the symmetrical samples used in previous experimental steps, the solar cells need to be doped with boron and phosphorous on each side. To isolate the backside of the cells, it was covered with a SiN_x capping layer. The samples were then doped with boron using the boron doping recipe previously used for the lifetime samples. The samples were then oxidized in the PECVD furnace with a previously optimized dry oxidation recipe (oxidation-650). Samples were dipped in an HF solution to etch the BSG layer formed on the front surface and the SiN_x capping layer on the back.

To protect the already doped boron emitter layer, the front side of the samples was covered with a PECVD SiN_x capping layer to avoid the neutralization of the boron emitter layer. The samples were then doped with phosphorous using POCl3 gas as a precursor.

The cells were then cleaned with the RCA method. For the passivation, the front side of the cells was passivated using the ALD device by layering it with an optimized thickness of 5 nm alumina (Al_2O_3) and SiN_x stack layer with a reflective index of 1.96. The backside was layered with the SiN_x ARC layer for passivation. Fabrication steps of Bifacial cells were identical to assess the reproducibility of the optimized methods.

Ultimately, the cells were screen printed with an H-grid mask using Ag/Al metal paste for the front and Ag paste for the backside metallization. They were then dried in a drying furnace and fired using a belt furnace. Two different temperatures of 855°C and 890°C were utilized on the samples. The J-V plot and other parameters such as the cell efficiency, Fill Factor, J_{sc} and Suns V_{oc} values were obtained using the solar simulator system. Figure 3.6 shows the fabrication steps of the bifacial cell.

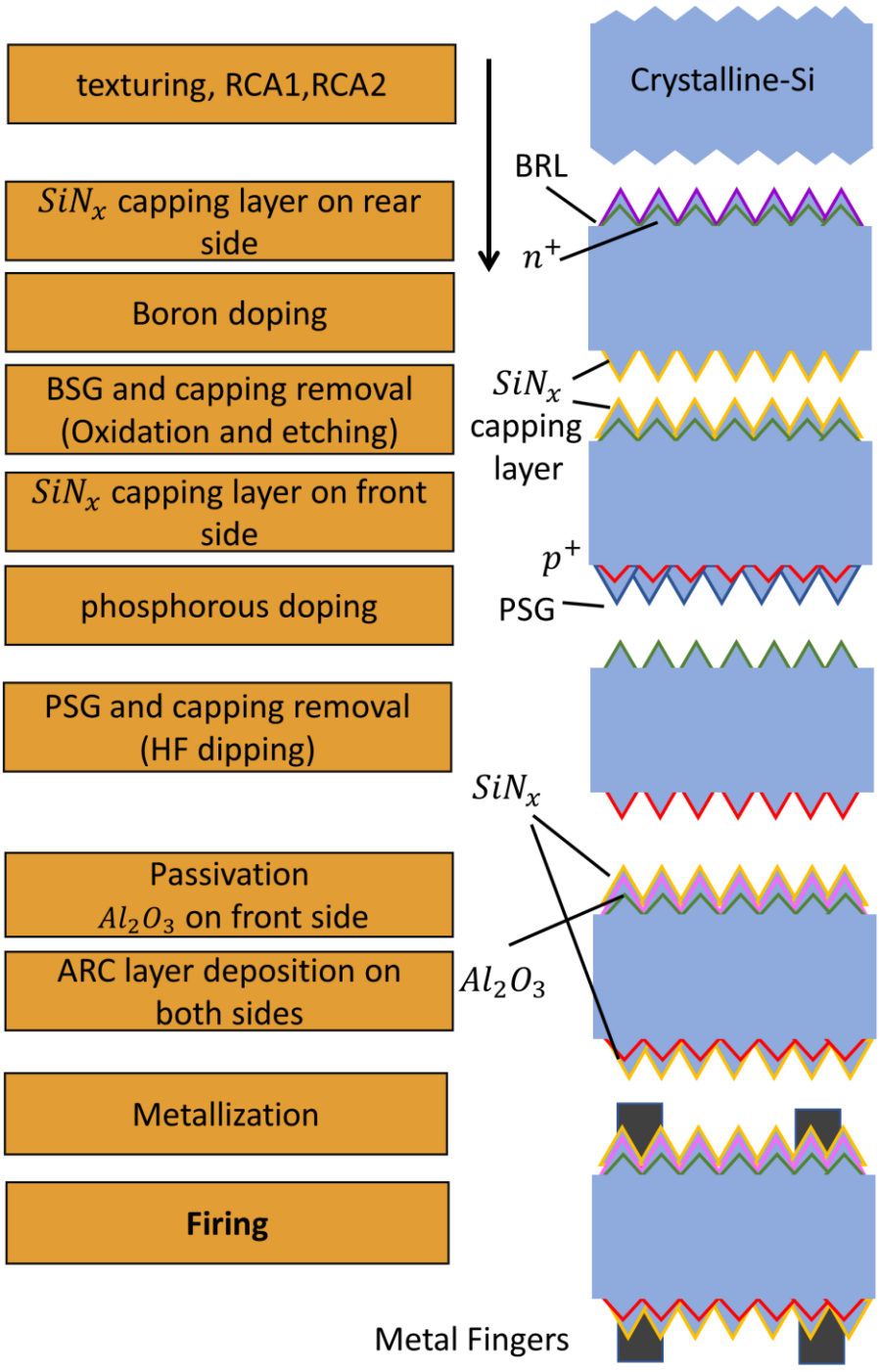

Figure 3.6. Flowchart and cross-section of fabrication steps of the Bifacial cells.

CHAPTER 4

RESULTS AND DISCUSSION

4.1 The First Set of Optimizations for The Boron Emitter Layer

Both n-type and p-type wafers were used in this experimental set were first textured and cleaned with the recipes previously optimized at the GÜNAM research center

4.1.1 Optimizations of the Oxidation Recipes

In the case of phosphorous doping, the PSG layer formed on the samples can easily be etched with an HF dip. However, in Boron diffusion, the samples are covered with a BRL layer that must be correctly oxidized before attempting to etch it. The samples were doped with a previously optimized boron diffusion recipe using BCl_3 as the precursor gas. Three different methods of oxidation have been utilized in this experiment. Pass3 and LTOnew are thermal oxidation, and RCA is a low-temperature chemical etching. The formed BSG layer was then etched away by dipping all the samples in a 10 percent HF solution for one minute.

The samples were measured using a four-point probe system to investigate the uniformity of boron doping and etching sheet resistance values, samples from each oxidation recipe were individually measured, and an average value was calculated from the measurements as plotted in Figure 4.1 and Figure 4.2.

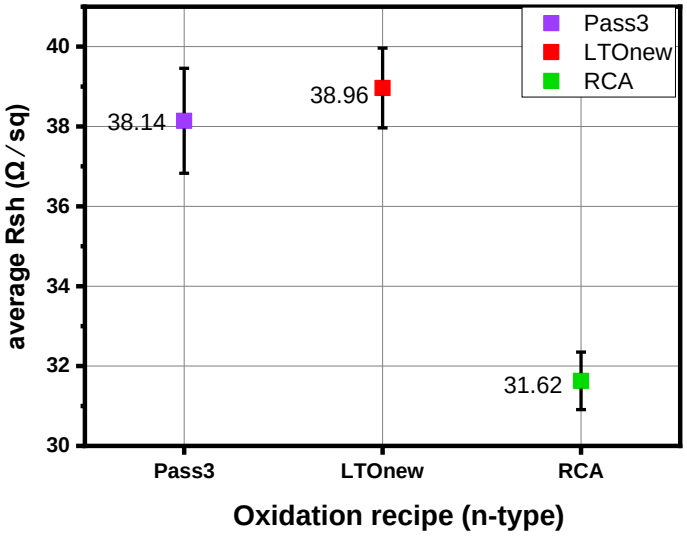

Figure 4.1. Average R_{sh} values for n-type samples.

The obtained sheet resistance values are in the range of 30-40 Ω/sq. As it is evident, the R_{sh} values for RCA samples are slightly lower compared to Pass3 & LTOnew. This could be due to the higher boron dopant concentrations on the surface of RCA, indicating that the BRL layer was not entirely removed.

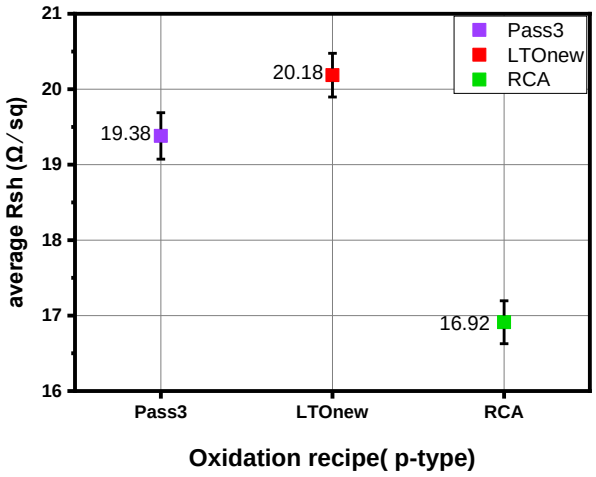

Figure 4.2. Average R_{sh} values for p-type samples.

Boron doping on p-type samples was investigated in this experimental set to assess the quality of the boron doping as a back surface field (BSF) layer. Sheet resistance values for the p-type samples are lower than the n-type values as expected, and are in the range of 15-20 Ω/sq.

The overall R_{sh} values for all samples from each oxidation recipe group values appeared to be close to each other in the range. In order to ensure uniformity of the doping, an R_{sh} mapping was carried out by taking the measurements on nine various sides of the samples, as marked in Figure 4.3.

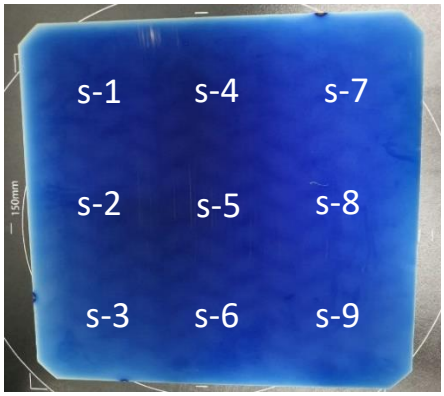

Figure 4.3. R_{sh} measurements were taken from the marked areas shown in this image.

The sheet resistance uniformity plots are shown in Figure 4.4.

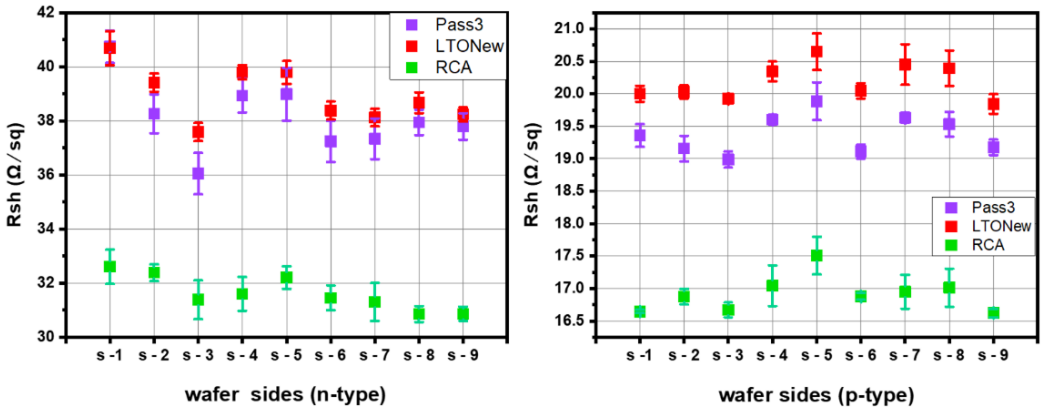

Figure 4.4. Uniformity check for the n-type and p-type lifetime samples.

All three oxidation samples show uniform R_{sh} values in all sides of the samples. This proves that the boron doping and the BRL layer removal were done uniformly across the samples for all three oxidation recipes. The dopant concentration was measured using the electrochemical capacitance-voltage (ECV) system to investigate the Boron doping concentration. The carrier concentration results are shown in Figure 4.5.

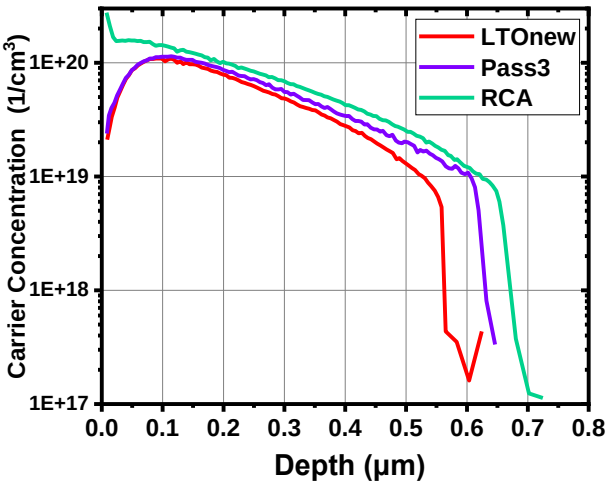

Figure 4.5. ECV results of oxidation recipes.

Both Pass3 and LTOnew oxidation samples had a peak doping concentration of $10^{20}cm^{-3}$. The penetration depth for Pass3 and LTOnew samples was around 0.6 um. There are around 70 nanometers of lower carrier concentration for both thermal oxidation recipes before it reaches its peak dopant concentration. This low carrier concentration value at the surface can be explained by a phenomenon called boron depletion. When the boron-rich layer is oxidized in an Oxygen-rich environment, Boron elements diffused in the area below the BRL layer tend to be oxidized rather than keeping their bond with Si atoms, resulting in the formation of this boron depleted region. This high depletion at the surface of our dry oxidation samples is required to be minimized to achieve higher efficiency and V_{oc} Values for our samples.

As for the RCA samples, the peak doping concentration is $2.76\times 10^{20}\ cm^{-3}$for the first ten nanometers at the surface and then drops to about $1.5\times 10^{20}cm^{-3}$. The penetration depth for the RCA sample was around 0.7 um. This high carrier concentration for the first ten nanometer of the surface can indicate insufficient oxidation for the chemical oxidation samples.

4.1.2 Optimization Works on the Passivation Layers

$Al_2O_3/\ SiN_x$ and $SiO_2/\ SiN_x$ stack passivation layers were used to passivate the lifetime samples. Two different Alumina thicknesses of 2 nm and 5nm were tested on the samples passivated with $Al_2O_3/\ SiN_x$ stack layer. Lifetime values were compared in Figure 4.6. The dashed lines are drawn as a visual aid.

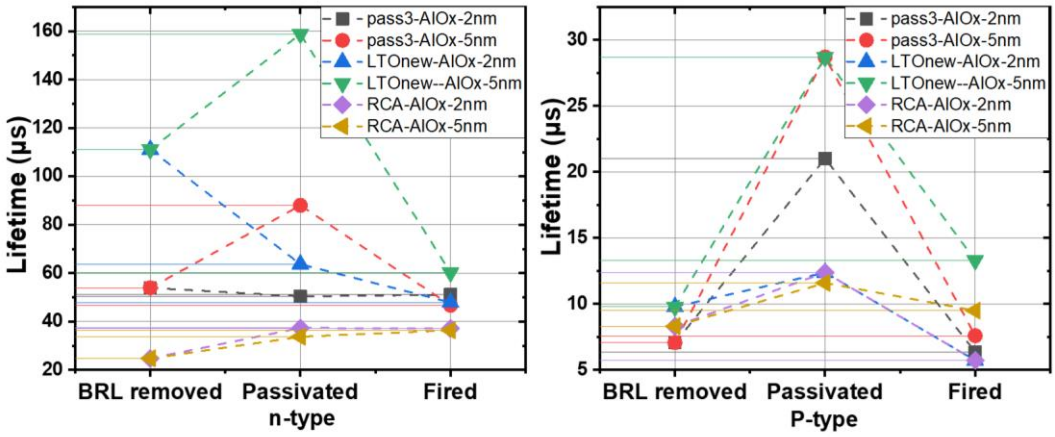

Figure 4.6. Comparison of lifetime results of passivated with 2nm and 5 nm Al_2O_3 for n-type and p-type samples.

For both n-type and p-type samples, thermal oxidation recipes showed promising improvement in lifetime after passivation with the alumina stack layer. However, firing the samples at 910° C caused the lifetime to drop significantly. The decrease in lifetime after firing in Al_2O_3 samples can be due to diffusion of hydrogen from SiN_x into the Al_2O_3 during the firing and causing blisters to appear on the surface. This blistering can be better observed in the PL images of the samples.

Generally, the 5 nm thick alumina appeared to be providing better passivation than the 2 nm thick alumina.

For the samples passivated with $SiO_2/\ SiN_x$ stack layer, two different SiN_x recipes (Sirich and Sirich3) were tested. Minority carrier lifetime results of the symmetrical samples are shown in Figure 4.7. The dashed lines are drawn as a visual aid.

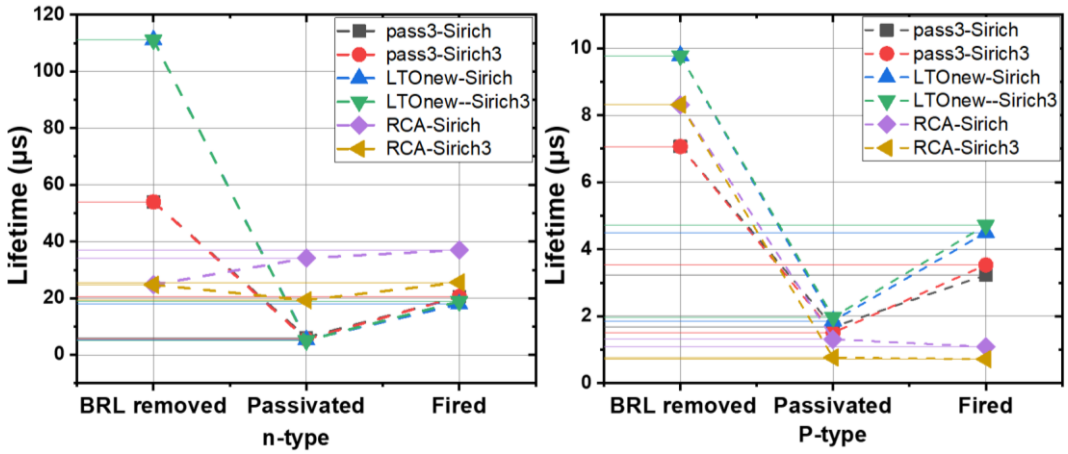

Figure 4.7. Comparison of lifetime results of Sirich and Sirich3 ARC layers in SiO_2 passivated n-type and p-type samples for all oxidation recipes.

it can be observed the lifetime values that the $SiO_2/\ SiN_x$ stack layer was not able to successfully passivate the lifetime samples. The lifetime drops significantly (from 110 µs to 8 µs) after the passivation layer deposition, and there seems to be no significant difference in passivation abilities of the Sirich and Sirch3 ARC layers.

Implied V_{oc} Values of all passivation recipes were compared in Figure 4.8. The dashed lines are drawn as a visual aid.

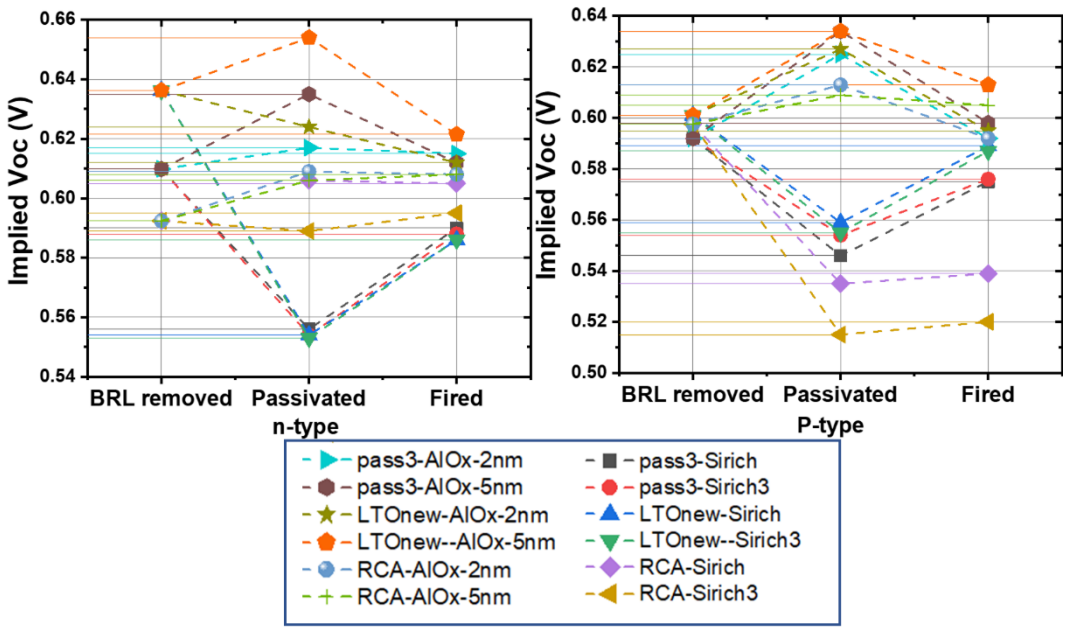

Figure 4.8. Comparison of impV_{oc} results of all samples.

For n-type samples, the samples passivated with $Al_2O_3/\ SiN_x$ show improved impV_{oc} values. However, they cannot maintain it during the firing, and the samples passivate with 5 nm alumina seem to be affected by the firing the most. Whereas the samples passivated with 2 nm alumina seem to withstand the effects of firing, especially the Pass3 oxidation recipe samples.

The impV_{oc} for the samples passivated with $SiO_2/\ SiN_x$ stack layer seems to drop after the passivation. However, the firing appears to be improving the passivation of the samples since the impV_{oc} values increase after the firing step. Overall, after comparing all the passivation recipes, the $Al_2O_3/\ SiN_x$ stack layer seems to have done a better job at passivating the samples than the $SiO_2/\ SiN_x$ stack layer.

The highest impV_{oc} value after firing was yielded by the LTOnew oxide recipe samples passivated by the $Al_2O_3/\ SiN_x$ stack layer. Imp V_{oc} values of 0.621 V and 0.613 V were obtained for the n-type and p-type samples, respectively, Figure 4.9, Figure 4.10, and Figure 4.11 show the before and after firing PL images of Pass3,

LTOnew, and RCA samples. It must be stated that some of the marks that have appeared on the after-firing PL images are from the speed belt of the firing furnace.

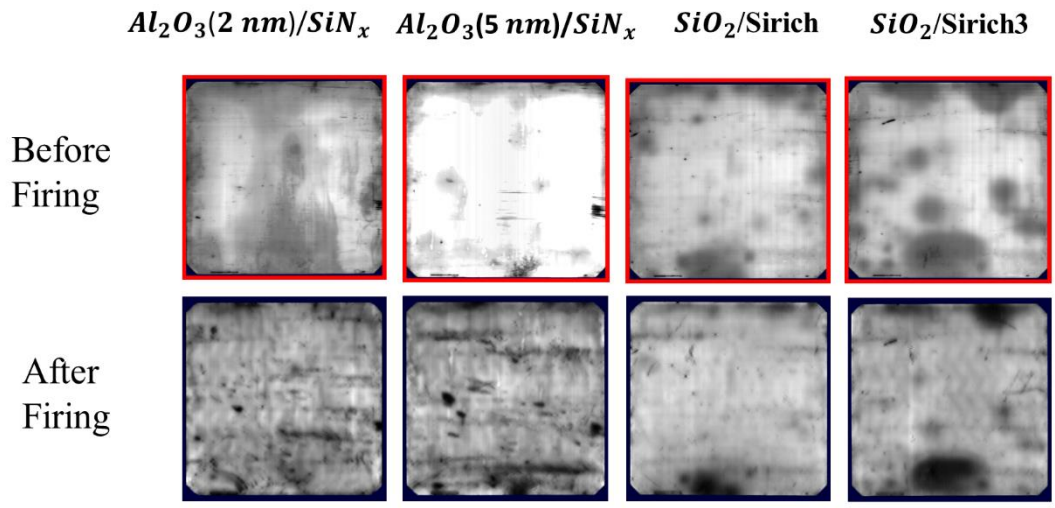

Figure 4.9. PL results of the Pass3 oxidation recipe.

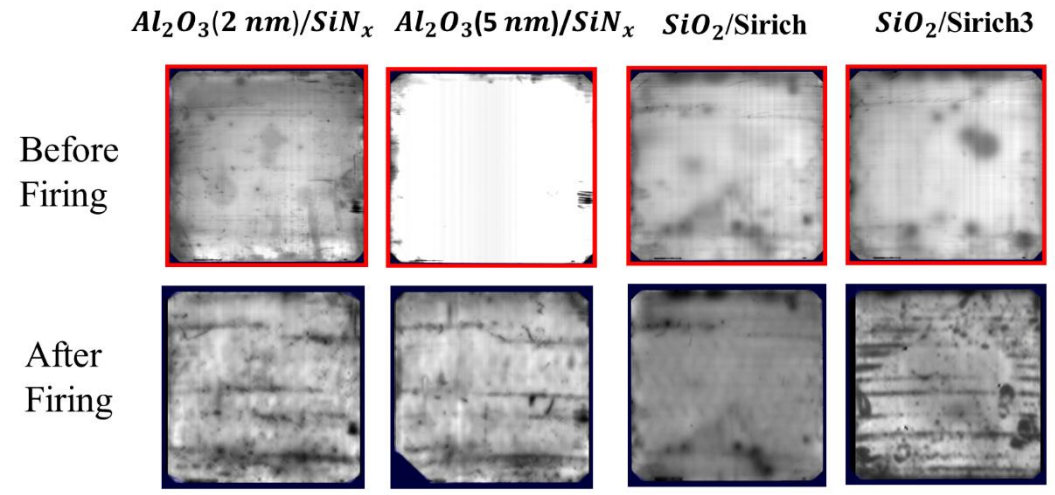

Figure 4.10. PL results of the LTOnew oxidation recipe.

some marks and blisterings have appeared on Al_2O_3 passivated thermal sample post-firing. This can be due to the diffusion of hydrogen from SiN_x into the Al_2O_3 causing blisters to appear on the sample's surface. It can be observed that the $SiO_2/\ SiN_x$ samples surface was not affected too much by the firing step. It can be noted from these images and the post-firing imp V_{oc} value improvement seen in Figure 4.8 that the the $SiO_2/\ SiN_x$ samples are more stable against firing.

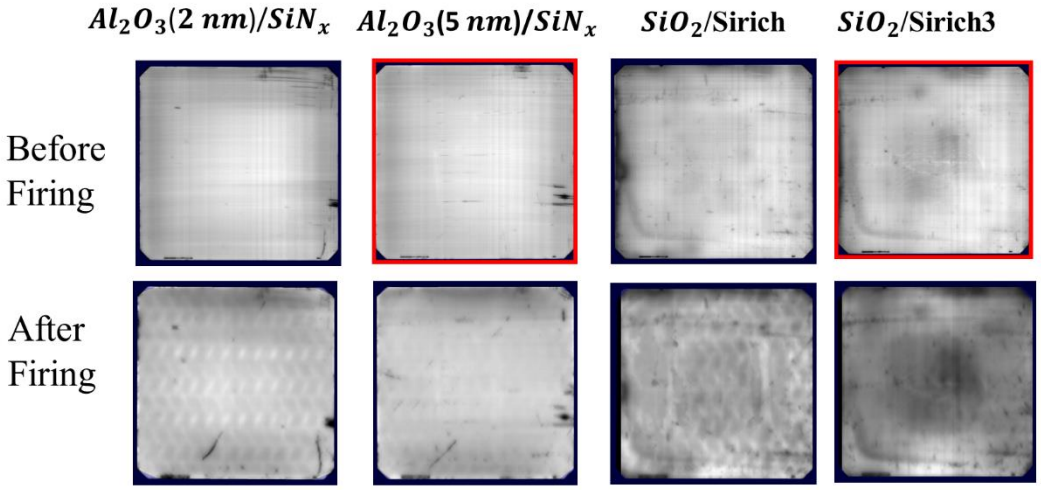

Figure 4.11. PL results of the RCA oxidation recipe.

It can be obtained from the pre-firing images of RCA oxide recipe samples that the samples appear to be more uniform and do not contain surface damage. This can be due to the fact that the samples are not exposed to high temperatures during oxidation. There is also no significant damage seen on the post-firing results as the before and after-firing ImpVoc results were almost constant.

4.1.3 Effect of Firing on Lifetime Samples

Figure 4.12 compares the carrier concentration of the samples measured before and after firing.

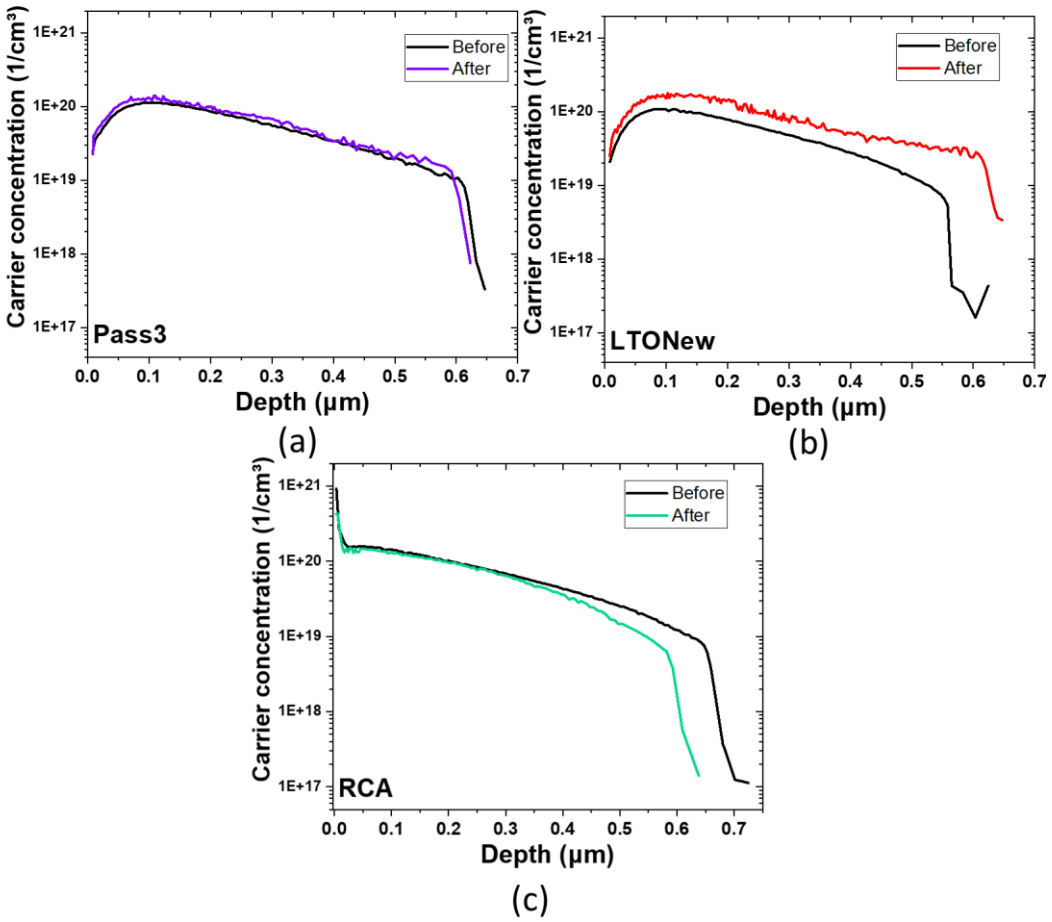

Figure 4.12. Comparison of Before and after firing ECV results for (a) Pass3 (b) LTOnew, and (c) RCA oxidation sets.

In thermal oxidation recipes, especially LTOnew, there seems to be an increase in carrier concentration and a slight increase in the penetration depth. However, in the RCA oxide recipe, the doping concentration appears to be stable at first; however, as the sample was further etched, a drop in the carrier concentration in the deeper areas of the emitter was observed.

4.1.4 TLM Measurements

In order to fabricate TLM samples, the symmetrical samples were screen printed with Al/Ag metal paste. The samples were then fired at different temperatures, and

TLM measurement was obtained. Contact resistivity of the samples is shown in Figure 4.13 and Figure 4.14.

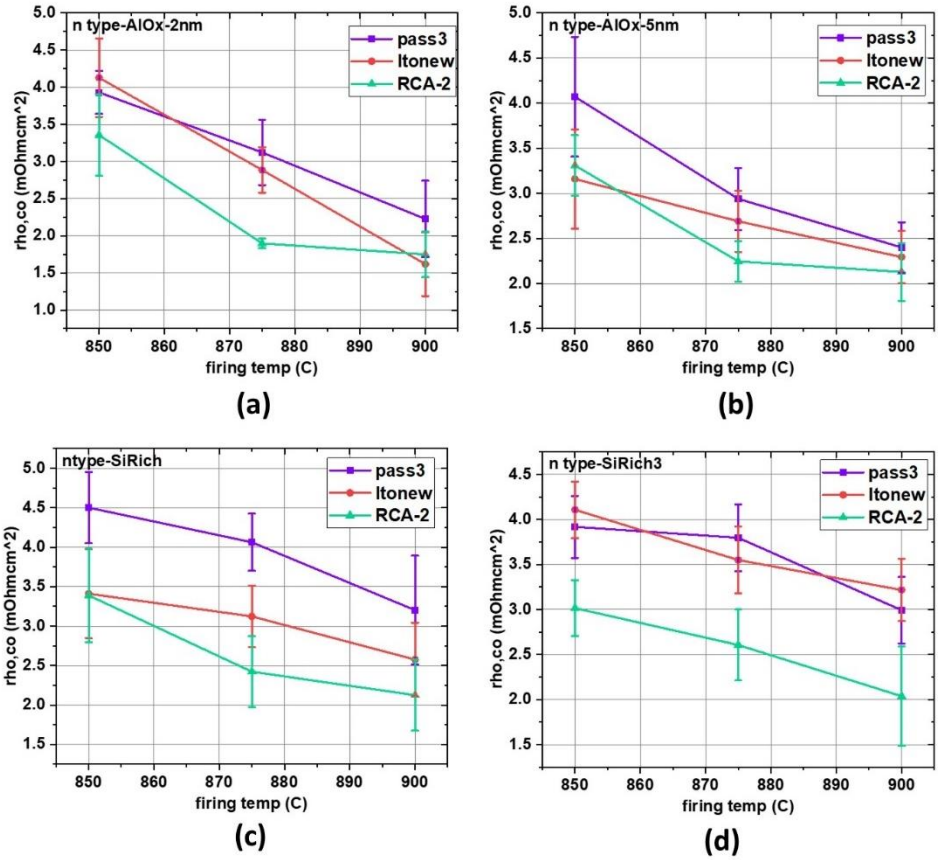

Figure 4.13. TLM results of n-type samples for (a) 2 nm Al_2O_3 /SiN_x stack layer (b) 5 nm Al_2O_3 /SiN_x stack layer (c) SiO_2 /SiN_x (Sirich recipe) (d) SiO_2 /SiN_x (Sirich3 recipe).

All three oxidation sets show fairly promising contact resistivity results. The results for the RCA samples show slightly lower contact resistivity than the high-temperature oxidation recipes. The contact resistivity in all passivation methods seems to be constant. Except for the Sirich3 ARC layer giving a very slightly lower contact resistivity compared to the Sirich recipe.

The overall behavior of contact resistivity versus temperature seems to have a descending pattern. The samples fired at 900° C give the lowest contact resistivity since the contact formation between the metal fingers and the semiconductor will improve with the firing temperature. However, there is a trade-off between low contact resistivity and high carrier lifetime. Since higher temperature can cause irreversible morphological damage to the cell structure, radically decreasing lifetime. Overall, contact resistivity in the range of 2-4 $m\Omega cm^2$ was obtained. Indicating that a good metal-semiconductor contact was formed. The lowest contact resistivity value obtained was 1.6 $m\Omega cm^2$ which was for the LTOnew oxide recipe with 2nm Al_2O_3/SiN_x stack layer.

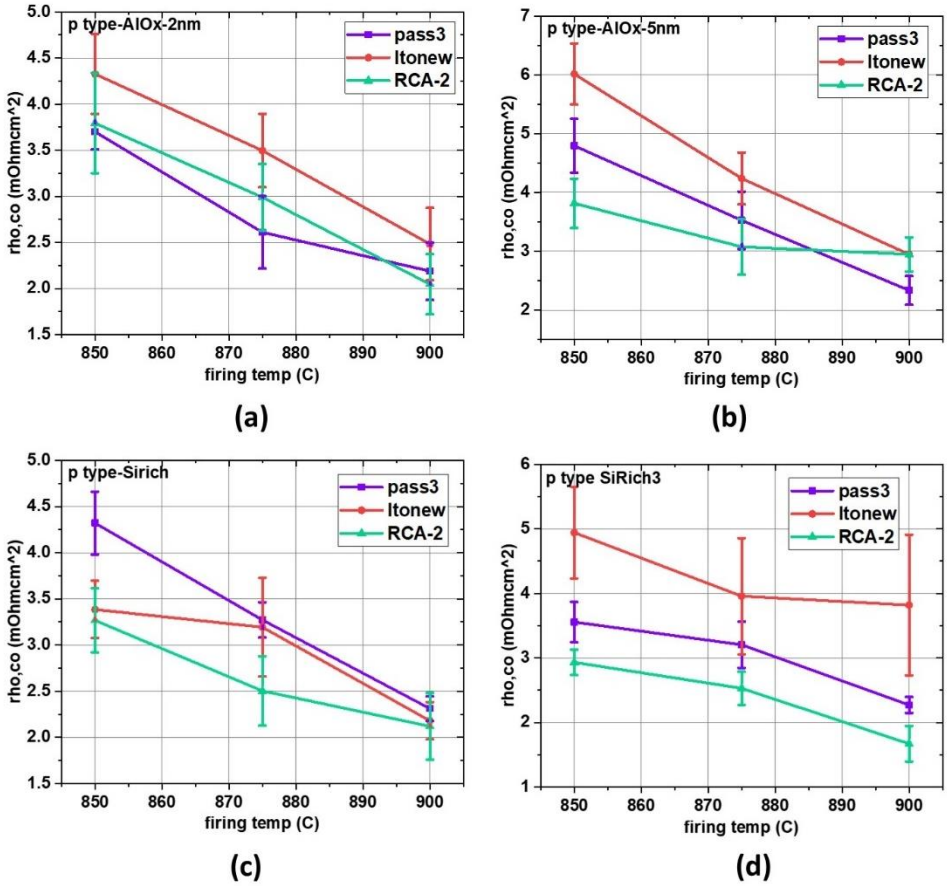

Figure 4.14. TLM results of p-type samples for (a) 2 nm Al_2O_3 /SiN_x stack layer (b) 5 nm Al_2O_3 /SiN_x stack layer (c) SiO_2 /SiN_x (Sirich recipe) (d) SiO_2 /SiN_x (Sirich3 recipe).

The p-type samples also obtained good contact resistivity values in the range of 3-6 $m\Omega cm^2$. Showing promising results for using the boron-doped layer as a BSF layer in P-type bifacial cells.

4.2 Second Optimization Tests

In this set, a different wet chemical oxidation recipe was optimized. Also, a low-temperature dry oxidation recipe was tested for the thermal oxidation process.

4.2.1 Chemical Oxidation Samples

A mixture of Nitric acid (HNO3), Acetic acid (CH3COOH), and Hydrofluoric acid (HF) were tested for the duration of 2, 3, 4, and 5 minutes. The ratio for each chemical component is shown in Table 4.1.

Table 4.1 Chemical ratio of the chemical oxidation recipe.

Chemicals	*ratio*
HNO3	100
CH3COOH	100
HF	1

The ECV results of the oxidation samples are shown in Figure 4.15.

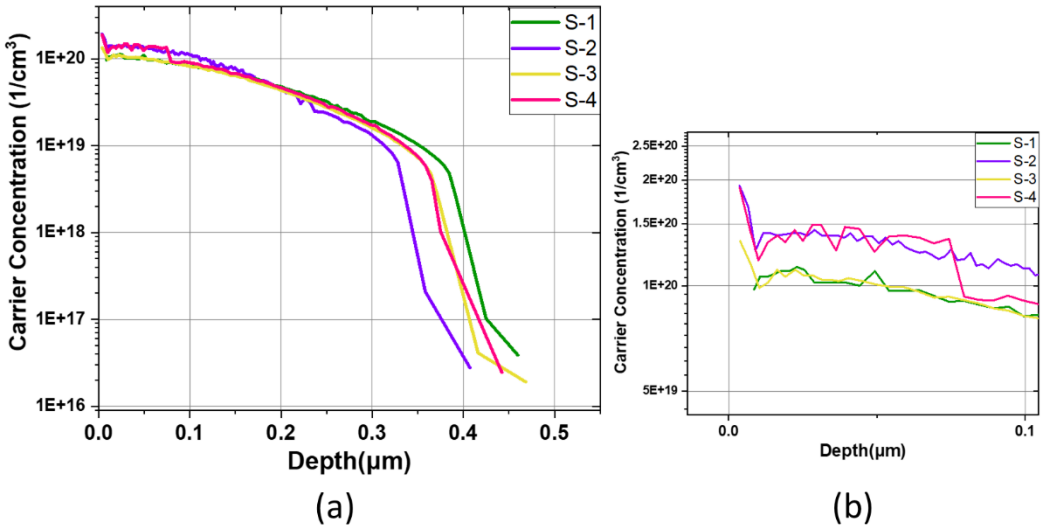

Figure 4.15. (a) ECV results of the Boron emitter layer (b) carrier concentration results of the emitter surface.

According to the ECV results, the chemical oxidation recipe successfully oxidized and etched the undesired boron-rich layer.

The ECV could not correctly measure the doping concentration in the first few nanometers of the sample etched for 2 min, which is probably to be due to high Carrier concentration. Around ten nanometers of the unetched boron-rich layer are visible on the surface of the samples etched for longer durations. However, this amount is considerably low compared to the RCA samples in the previous experimental set. The characterization results of the oxide samples are shown in Table 4.2.

Table 4.2 characterization results of oxidation samples

Oxidation samples	*Oxidation Duration(min)*	*Sheet resistance Values (Ω/sq)*	*Lifetime (us)*	*Imp Voc (V)*
S-1	2	53.50	48.61	0.606
S-2	3	57.06	29.43	0.593
S-3	4	54.50	44.50	0.604
S-4	5	55.71	33.53	0.596

The R_{sh} values were measured on both sides of the samples using the 4PP device. And the lifetime and impV_{oc} were obtained using the Sinton device. All the oxidation samples yield relatively uniform sheet resistance values, which indicates that the samples were all oxidized and etched uniformly. The impV_{oc} values alter slightly with each increase in duration but are still in acceptable ranges. Later, a diluted version of this chemical solution was tried with the ratios seen in Table 4.3.

Table 4.3 Diluted chemical ratio of the chemical oxidation recipe.

Chemicals	Ratio
HNO3	90
CH3COOH	90
HF	20
H_2O	800

The oxidation test samples were dipped in the diluted solution for 10 and 22 minutes. The doping profile of the diluted chemical oxidation recipe samples was then measured with ECV, as shown in Figure 4.16, and the characterization results of the diluted chemical oxidation recipe are shown in Table 4.4:

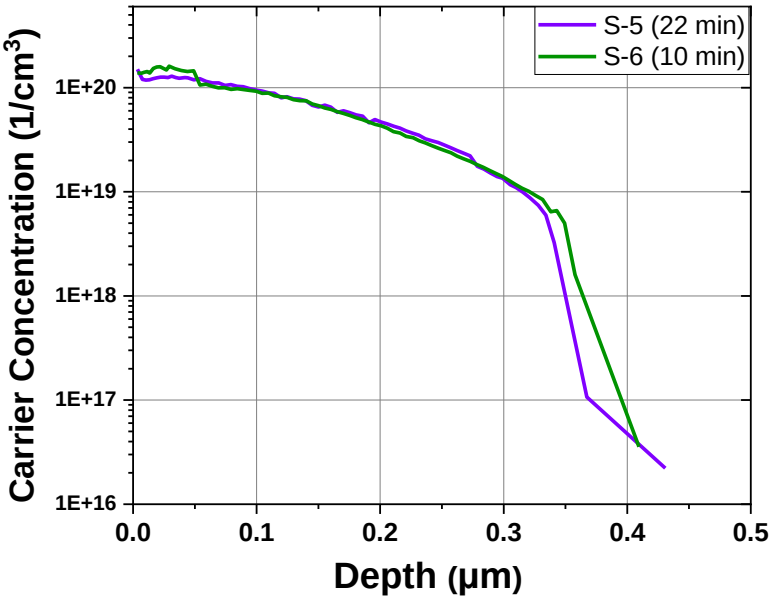

Figure 4.16. Carrier concentration results of different durations.

Table 4.4 Characterization results of diluted chemical oxidation samples.

Oxidation samples	*Oxidation Duration(min)*	*Lifetime (us)*	*Imp Voc (V)*
S-6	10	41.07	0.601
S-5	22	39.59	0.602

The ECV results show that the diluted recipe can thoroughly remove the BRL layer by increasing the oxidation duration. They yielded a peak carrier concentration of $1.43\times 10^{20}\ cm^{-3}$ with a junction depth of 0.4 μm. Overall, both etching duration for the samples appear to yield similar impV_{oc} Results. A duration of 10 minutes seems to be a good choice since it is preferred to minimize the sample's exposure to harmful chemicals. However, because the lifetime samples are full-size wafers, the lifetime samples were oxidized for 16 minutes to ensure completed oxidation.

4.2.2 Lifetime Samples

The lifetime samples were oxidized using two different oxidation recipes. set-1 samples were oxidized by the chemical oxidation tested on the small-sized samples in the previous section. Set-2 samples were oxidized with a dry oxidation recipe. The gas flow for this dry oxidation was the same as Pass3 samples in the first experiment. However, the temperature was lowered from 850°C to 650 °C. One of the previously cut small samples was also oxidized with the batch for ECV measurements.

Carrier concentration results of all three ECV samples with no oxidation, low thermal oxidation, and chemical oxidation were compared in Figure 4.17.

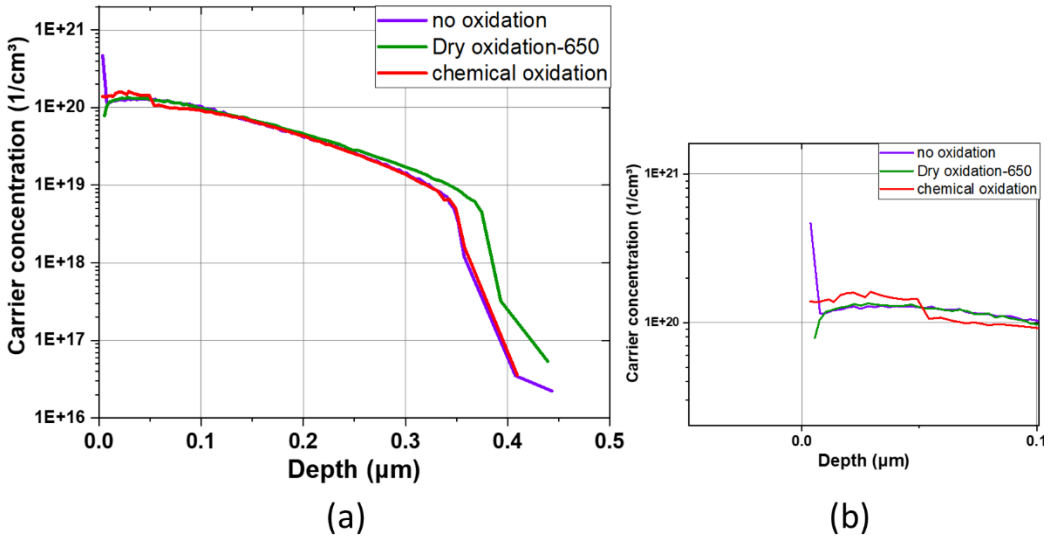

Figure 4.17. (a) ECV results of the Boron emitter layer (b) Carrier concentration results of the emitter surface in the first 100 nm.

As can be seen in part (b), the carrier concentration of the unoxidized sample surface is very high (peak carrier concentration of $4.87\times 10^{20}\ cm^{-3}$). it can be attributed to the unoxidized BRL on the surface.

However, the oxidation of other samples has been successfully done since the surfaces seem to be devoid of any boron-rich layer. The low thermal oxidation

samples have a small boron depleted region at the surface of around 10 nm with the carrier concentration $7.89 \times 10^{19}\ cm^{-3}$. However, the amount is negligible and can contribute to the emitter layer passivation. the peak carrier concentration for low thermal oxidation was $1.35\times 10^{20}\ cm^{-3}$.

The chemical oxidation recipe also did a great job of oxidizing and eliminating the BRL layer on the surface, as discussed in Figure 4.16.

Oxidized samples were then etched and cleaned. Carrier lifetime and impV_{oc} of the samples was measured using the Sinton QSSPC lifetime measurement device. The cleaned samples were passivated with 2nm thick Al_2O_3/SiN_x stack layer. Two recipes were used for the SiN_x layer. Pass4 with a refractive index of 1.96 and Pass5 with a refractive index of 1.73 was tested on the lifetime samples.

passivated samples were fired at three different temperatures of 850°, 880°, and 910° C to test the effect of firing on the sample's lifetime and impV_{oc}. The before and after firing results were then compared as depicted in the plots shown in Figure 4.18. The dashed lines are drawn as visual aid.

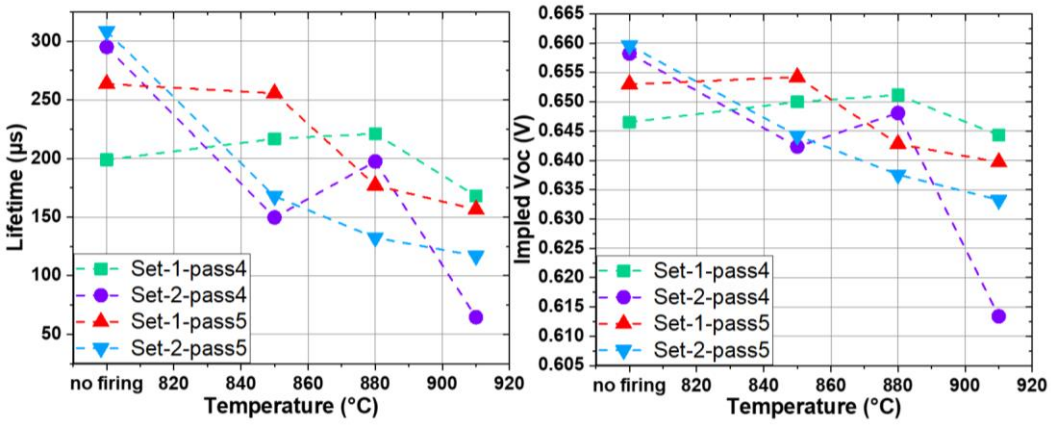

Figure 4.18. Comparison of the before firing and after firing $impV_{oc}$ and lifetime results of passivated samples.

the effects of firing on the minority carrier's lifetime and impV_{oc} can be observed. As it can be understood from the plots, as the firing temperature increases, the minority carrier lifetime and impV_{oc} values deteriorate. However, it is an unavoidable step of metallization to ensure that the metal-semiconductor contact will be effectively formed. Thermal oxidation (set-2) samples have a higher lifetime and impV_{oc} values than Wet chemical oxidation (Set-1) samples. However, the set-2 values plummet when exposed to high temperatures. Set-1 samples show better endurance to heat. It could be assumed that since the thermal oxidation samples were already exposed to high temperatures once, the second extreme exposure to heat can cause further damage.

For chemical oxide recipes, best passivation was achieved for the pass4 passivation layer and firing temperature of 880°C with a minority carrier lifetime of 221 μs and impV_{oc} of 0.651 V. for the low thermal oxide recipe, the best passivation was again achieved with a pass4 passivation layer and firing temperature of 880°C with a minority carrier lifetime of 197.5 μs and imp V_{oc} of 0.648 V.

Pass5 passivation samples seem to have a lower tolerance to firing temperature since best results was achieved by the samples fired at 850°C, and the values seem to drop as the temperature increases.

Finally, the results of the previous experimental set with 2nm Al_2O_3/SiN_x passivation layer and the current samples were compared for different fabrication steps. Figure 4.19. shows the comparison of lifetime and imp V_{oc} results.

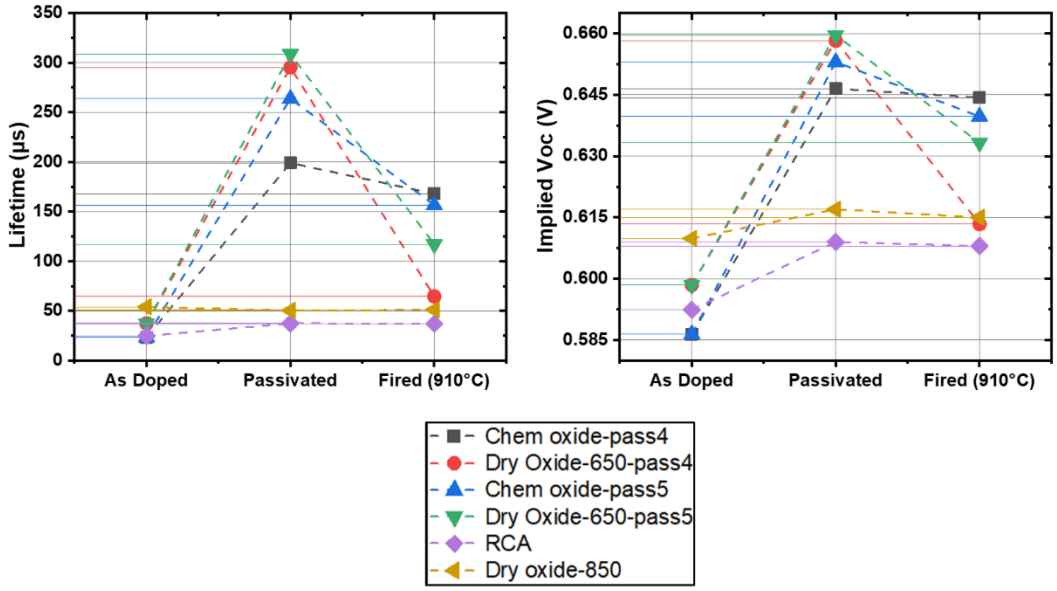

Figure 4.19. Lifetime and Implied V_{oc} result comparison of first and second optimization experiments.

The as doped carrier lifetime results are close to each other. However, there is an evident improvement in the passivated sample values in the second experiment set compared to the first set. By reducing the oxidation temperature for the same gas flow recipe, we were able to increase the imp V_{oc} by 41 mV, and the lifetime by 240 µs. The chemical oxidation results had also improved significantly compared to the RCA sample. The imp V_{oc} and lifetime of the passivated samples were increased by 49 mV and 258 µs, respectively.

The second set was still affected a lot by the high firing temperatures. However, by lowering the firing temperature to around 880°C, we will be able to keep the passivating properties intact.

4.2.3 TLM Samples

The TLM samples were prepared by printing the lifetime samples with metal grids on one side. They were then fired at two different temperatures (880°and 900° C) in order to investigate the effect of firing temperature alteration on the junction formation and contact resistivity of lifetime samples. TLM measurement method was used to measure the contact resistivity of the samples. The contact resistivity results are shown in Table 4.5.

Table 4.5 Contact resistivity values of samples fired at two temperatures.

Sample name	*880*° C	*900*° C
set-1-Pass4	6.3$\pm$1.2	4.8$\pm$0.9
set-1-Pass5	5.5$\pm$0.8	3.7 $\pm$ 0.9
set-2-Pass4	6.3$\pm$1.2	4.5$\pm$0.9
set-2-Pass5	4.7$\pm$0.9	3.5$\pm$0.8

The 900° C firing temperature samples yielded a lower contact resistivity value of around 3.5-5 $m\Omega cm^2$ however, as observed in Figure 4.18, the passivation qualities of the samples seriously deteriorated at this temperature. Therefore, the firing temperature of 880° C seems to be suitable for firing since its effect on the impV_{oc} was minimal and a reasonably good establishing a good contact between the metal fingers and semiconductor were formed. The contact resistivity values were in the range of 4.5-6.5 $m\Omega cm^2$.

4.3 Cell production

This study aims to improve the lifetime of carriers in the emitter layer of crystalline wafers to manufacture an efficient bifacial solar cell. A set of n-type bifacial solar cells were produced to finalize the optimization of the emitter layer and test the obtained optimization results. The samples were doped with Boron and phosphorous.

Samples were oxidized with a previously optimized dry oxidation recipe (oxidation-650). For passivation, the samples were layered with 5 nm thick alumina (Al_2O_3) and SiN_x stack layer with a reflective index of 1.96 (pass4). The backside was layered with the SiN_x ARC layer.

Finally, using Ag/Al metal paste for the front and Ag paste for the backside, H-grid pattern fingers and busbars were screen-printed on both sides of the cells, and samples were fired at two different temperatures. The first two samples were fired at 855°C and the rest was fired at 890°C. The J-V plot and other parameters such as the cell efficiency, Fill Factor, J_{sc} and Suns V_{oc} values were obtained using the solar simulator system. All cells were fabricated identically to assess the reproducibility of the optimized methods. Table 4.6 and Table 4.7 show the efficiency results of all 12 produced cells measured on the front and rear sides obtained from the solar simulator system.

Table 4.6 I-V results of the front side of Bifacial cells obtained from the solar simulator. The highest values for each column are marked with green markers.

Cell number	η [%]	FF [%]	Jsc [mA/cm²]	V_{oc} [V]
#1	17.3	76.5	35.8	0.631
#2	17.4	76.8	36	0.631
#3	18.1	79.6	36.1	0.630
#4	18.1	79.8	36	0.630
#5	17.6	78.3	35.7	0.629
#6	17.8	79	35.9	0.630
#7	17.8	77.8	36.2	0.632
#8	17.9	78.3	36.2	0.633
#9	17.9	78.5	36.1	0.632
#10	17.8	78.7	35.9	0.631
#11	18.2	80.2	35.9	0.631
#12	18.2	80.1	35.9	0.631

Table 4.7 I-V results of the rear side of Bifacial cells obtained from the solar simulator. The highest values for each column are marked with green markers.

Cell number	η [%]	FF [%]	Jsc [mA/cm²]	V_{oc} [V]
#1	15.8	76.8	32.7	0.629
#2	15.8	77.4	32.6	0.627
#3	16.1	79	32.4	0.627
#4	16.2	79.4	32.4	0.628
#5	15.6	78.3	31.8	0.626
#6	15.8	79.1	31.9	0.626
#7	16	77.9	32.7	0.629
#8	16	78	32.6	0.630
#9	16	79	32.2	0.629
#10	15.8	78.9	31.9	0.627
#11	16	80.1	31.8	0.628

#12	16	80	31.8	0.627

The first two samples fired at 855° C were observed to have lower FF values because the low firing temperature has failed to establish good metal-semiconductor contact. Overall the results show relatively constant FF and V_{oc} values, affirming the reproducibility of the optimized fabrication steps. The J-V plot for the best-performing cell is shown in Figure 4.20.

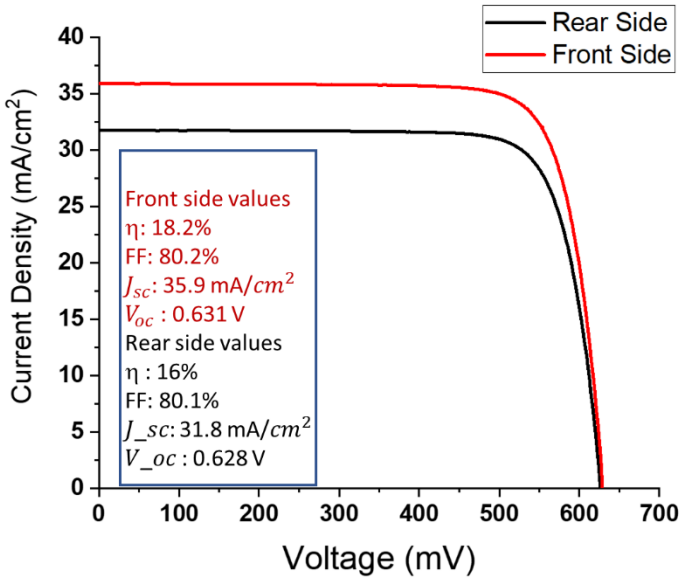

Figure 4.20. The J-V results of the best-performing cell.

The best bifacial cell fabricated with the optimized emitter layer yielded 18.2% efficiency on the front side and 16% efficiency on the rear side. The Bifaciality factor of the cell is 87.9%.

CHAPTER 5

CONCLUSION

With the current worldwide Energy crisis, producing clean and renewable energies has gained importance more than ever. Solar energy is one of the most outstanding options among renewable energies, offering a clean, cost-effective, and abundant energy source. The most widely used material in fabricating solar cells is silicon. P-type silicon is the commonly used silicon type according to industrial records. However, there has been an ongoing interest in n-type silicon in the past decade. Compared to p-type cells, n-type cells yield better efficiency and lifetime values and are unaffected by boron-oxygen defect and light-induced degradation (LID).

The many advantages that the n-type cells hold against p-type cells are the reason behind the ever-increasing interest in n-type wafers despite the p-type cell’s current dominance in the industry. According to the ITRPV's estimation, the n-type cell structures will be taking half the industry's share by 2031 [16]. However, the processes of boron emitter doping and passivation in this cell type can be challenging. Also, a boron-rich layer (BRL) forms during the boron doping process. Due to the high density of inactive boron atoms, BRL acts as a high carrier recombination site. As a result, it is essential to effectively remove and replace with another layer that effectively passivates the emitter surface. Therefore, the primary aim of this thesis was to optimize the boron doping recipe resulting in uniformly doped emitter regions. Industrially feasible methods for the fabrication of n-type silicon solar cells with front-side boron-doped emitters were implemented and assessed in this thesis work. Utilizing these optimized layers made it possible to fabricate efficient bifacial n-type silicon solar cells.

In the first set of optimizations, several thermal and chemical oxidation recipes were tested to eliminate the BRL successfully. The peak carrier concentration of

$10^{20}\ cm^{-3}$ and a penetration depth of 0.6 μm was obtained for the thermal oxidation recipes. the RCA recipe yielded a peak carrier concentration of $2.76 \times 10^{20}\ cm^{-3}$ and a penetration depth of 0.7 μm. This high peak concentration is believed to be due to the BSG layer remnants that weren't entirely removed during the oxidation process.

The samples were passivated with $Al_2O_3\ /SiN_x$ stack Layers with two different Alumina thicknesses of 2 and 5 nm. SiO_2/SiN_x passivation stack layer was also tested by utilizing two different SiN_x recipes. the tested samples were then fired, the highest imp V_{oc} values measured for n-type and p-type cells were 0.621 V and 0.613 V, respectively. Both of these results belong to the LTOnew oxide recipe samples passivated with 5 nm thick $Al_2O_3\ /SiN_x$ stack Layer. the SiO_2/SiN_x stack layer failed to passivate the cells successfully. However, by comparing the before and after firing impV_{oc} results, it was observed that the Alumina samples could not withstand the high firing temperature. impV_{oc} values of Alumina samples plummets after the firing, especially the 5nm thick samples. The samples were then metalized and fired again. Good contact resistivity in the range of 2-4 mΩcm^2 were obtained for the n-type samples.

In the second optimization, a new chemical oxide recipe was tested aiming to optimize a chemical oxidation recipe that would effectively oxidize and etch the BRL layer. We achieved a peak carrier concentration of $1.43\times 10^{20}\ cm^{-3}$ and penetration depth of 0.4 μm. Also, we focused on optimizing a dry oxide recipe with a lower temperature of 650°C to help maintain the minority carrier lifetime and impV_{oc} values of our samples. the dry oxidation samples yielded a peak carrier concentration of $1.35\times 10^{20} cm^{-3}$ and a penetration depth of 0.4 μm. the samples were passivated with 2 nm thick $Al_2O_3\ /SiN_x$ layers. Two different SiN_x recipes were tested for this passivation layer. The best results for both oxide recipes were achieved for the Pass4 passivation recipe and 880°C firing temperature. The chemical oxide recipe samples yielded an impV_{oc} of 0.651 V, and the Dry oxidation yielded an impV_{oc} of 0.648 V. the contact resistivities for the TLM samples were in the range of 4.5-6.5 mΩcm^2.

Lastly, using all of the optimizations, bifacial solar cells were fabricated. The best-performing bifacial cell yielded an efficiency of 18.2%, with a V_{oc} of 0.631 V, J_{sc} of 35.9 mA/cm2 and a FF of 80.2 % on the front side. Overall, we could utilize the optimizations developed in this work to make a fully functioning Bifacial solar cell with high reproducibility.

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